advanced electronic systems

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Lectures, tutorials and labs

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Damien PRÊLE
prele@apc.in2p3.fr

Contents

I Filters 7

1 Filters 9
- 1.1 Introduction . . . 9
- 1.2 Filter parameters . . . 9
  - 1.2.1 Voltage transfer function . . . 9
  - 1.2.2 S plane (Laplace domain) . . . 11
  - 1.2.3 Bode plot (Fourier domain) . . . 12
- 1.3 Cascading filter stages . . . 16
  - 1.3.1 Polynomial equations . . . 17
  - 1.3.2 Filter Tables . . . 20
  - 1.3.3 The use of filter tables . . . 22
  - 1.3.4 Conversion from low-pass filter . . . 23
- 1.4 Filter synthesis . . . 25
  - 1.4.1 Sallen-Key topology . . . 25
- 1.5 Amplitude responses . . . 28
  - 1.5.1 Filter specifications . . . 28
  - 1.5.2 Amplitude response curves . . . 29
- 1.6 Switched capacitor filters . . . 33
  - 1.6.1 Switched capacitor . . . 33
  - 1.6.2 Switched capacitor filters . . . 34

Tutorial 37
- 1.7 First order passive filter . . . 37
- 1.8 Second order passive filter . . . 38
- 1.9 Active filter - Sallen-Key topology . . . 38
- 1.10 5^{th} order Butterworth low-pass filter . . . 39
- 1.11 4^{th} order Chebyshev (3dB) low-pass filter . . . 39
- 1.12 6^{th} order Bessel high-pass filter . . . 39
- 1.13 Filter synthesis from template . . . 39
  - 1.13.1 Low pass-filter synthesis . . . 39
  - 1.13.2 Removing harmonics frequencies . . . 40

Lab 41
- 1.14 Passive filter . . . 41
- 1.15 Low pass-filter synthesis . . . 42
- 1.16 Removing harmonics frequencies . . . 43

II DCDC Converters **45**

2 DC/DC converters **47**
2.1 Introduction . . . 47
2.1.1 Advantages/Disadvantages . . . 47
2.1.2 Applications . . . 48
2.2 DC/DC converters . . . 48
2.2.1 *Buck* converters . . . 49
2.2.2 *Boost* converters . . . 50
2.2.3 *Buck-boost* inverting converters . . . 52
2.2.4 *Flyback* converters . . . 53
2.3 Control . . . 54
2.3.1 Feedback regulation . . . 54
2.3.2 Voltage regulation . . . 54

Tutorial **56**
2.4 DC/DC converter and duty cycle . . . 57
2.5 Triangle wave oscillator for PWM . . . 57
2.6 Preparation of the practical work . . . 58
2.6.1 Triangle wave oscillator under a single V_{CC} power supply . . . 58
2.6.2 Comparator . . . 59
2.6.3 Switching transistor . . . 59
2.6.4 DC/DC *buck* converter . . . 60
2.6.5 Voltage regulation . . . 60

Lab **63**
2.7 Pulse Width Modulation (PWM) . . . 63
2.8 Transistor driver . . . 64
2.9 Waveform signals in a *buck* converter . . . 64
2.10 Voltage regulation . . . 65

III Phase Locked Loop **67**

3 Phase Locked Loop **69**
3.1 Introduction . . . 69
3.2 Description . . . 69
3.2.1 Phase detector/comparator . . . 70
3.2.2 Voltage Control Oscillator - VCO . . . 73
3.3 Frequency range . . . 74
3.3.1 Lock range $2\Delta f_L$ . . . 74
3.3.2 Capture range $2\Delta f_C$ . . . 75
3.4 Frequency response . . . 76
3.4.1 One pole loop filter . . . 77
3.4.2 One pole - one zero loop filter (like PID) . . . 77

Tutorial **79**
3.5 Frequency Shift Keying (FSK) demodulation . . . 79
3.5.1 VCO setting . . . 80
3.5.2 Loop filter and PLL response . . . 80
3.6 PLL as a frequency multiplier . . . 81
3.6.1 PLL with one pole - one zero loop filter . . . 81
3.6.2 Loop with multiplication . . . 82
3.6.3 Frequency synthesizes . . . 83

Lab **84**
3.7 Frequency Shift Keying (FSK) demodulation . . . 85
3.7.1 FSK demodulation using a CD4046 PLL . . . 85
3.7.2 Frequency Shift Keying (FSK) signal using the function generator . . . 86
3.8 Frequency multiplier . . . 87
3.8.1 PLL with one pole - one zero loop filter . . . 87
3.8.2 Loop with multiplication . . . 87
3.8.3 Frequency synthesizes . . . 88

IV Modulation **91**

4 Modulation **93**
4.1 Introduction . . . 93
4.2 Amplitude modulation . . . 94
4.2.1 Modulation index . . . 96
4.3 Amplitude demodulation . . . 97
4.3.1 Envelope demodulation . . . 97
4.3.2 Product demodulation . . . 99

Tutorial **105**
4.4 Double Side Bande Amplitude Modulation . . . 105
4.4.1 Modulation without carrier transmission . . . 105
4.4.2 The use of an AD633 as multiplier . . . 106
4.4.3 Product detection . . . 106
4.4.4 Modulation with carrier transmission using an AD633 . . . 106
4.4.5 Modulation index adjustment . . . 107
4.4.6 Enveloppe detection . . . 107

Lab **109**
4.5 Amplitude modulation as a simple multiplication . . . 109
4.5.1 Modulation . . . 109
4.5.2 Product detection . . . 110
4.5.3 Modulation with adding carrier . . . 110
4.5.4 Envelope detection . . . 111

A Polynomials filter tables **113**

B Frequency response of polynomial filters **115**

C Angles, sin **and** cos **transformation formulas** **121**

D TL081 Data Sheet **123**

E LM311 Data Sheet **125**

F Zener diodes Data Sheet **127**

G BDX54 Data Sheet **129**

H Rectifier Data Sheet **131**

I LM158 Data Sheet **133**

J CD4046 Data Sheet **135**

K CD4018 Data Sheet **141**

L AD633 Data Sheet **143**

M Signal diode Data Sheet **149**

N 78XX Linear voltage regulator Data Sheet **151**

Foreword

THE present document is based on four lectures given for Master of Space and Aeronautics in University of Science and Technology of Hanoi. It consists of four parts. The first one is devoted to **filters**, while the second one deals with **DC/DC converter**, the third one discusses the **phase locked loop** and the last the **modulation**. For convenience of the readers the work is organized so that each part is self-contained and can be read independently. These four electronic systems are chosen because they are representative of critical elements encountered in spacecraft; wether for power supply or for data transmission.

Acknowledgements : Damien Prêle was teaching assistants in Paris-6 University for 4 years with professor Michel REDON. Topics of this lecture are inspired from M. Redon's lectures given at Paris-6 University for electronic masters. Therefore, this lecture is dedicated to the memory of professor Michel REDON who gave to the author his understanding of the electronic and helped him to start teaching it.

Moreover, the author would like to express his gratitude to Miss Nguyen Phuong Mai and Mr. Pham Ngoc Dong for their help for the preparation of this teaching in the University of Science and Technology of Hanoi.

Part I

Filters

1 Filters

1.1 Introduction

A filter performs a **frequency-dependent signal processing**. A filter is generally used to select a useful frequency band out from a wide band signal (example : to isolate station in radio receiver). It is also used to remove unwanted parasitic frequency band (example : rejection of the 50-60 Hz line frequency or DC blocking). Analogue to digital converter also require anti-aliasing low-pass filters.

The most common filters are low-pass, high-pass, band-pass and band-stop (or notch if the rejection band is narrow) filters :

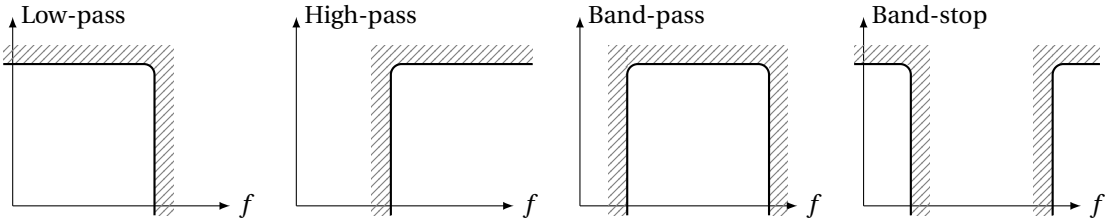


Figure 1.1: Transfer function of ideal filter : Fixed gain in the pass band and zero gain everywhere else ; transition at the cutoff frequency.

To do an electronic filter, **devices which have frequency-dependent electric parameter as L and C impedances** are required. The use of these reactive impedances* into a voltage bridge is the most common method to do a filtering ; this is called passive filtering. **Passive (R,L,C) filter is used at high frequencies** due to the low L and C values required. But, **at frequency lower than 1 MHz, it is more common to use active filters made by an operational amplifier** in addition to R and C with reasonable values. Furthermore, active filter parameters are less affected† by load impedances than passive one.

1.2 Filter parameters

1.2.1 Voltage transfer function

Passive low-pass filter example : a first order low-pass filter is made by R-C or L-R circuit as a voltage divider with frequency-dependent impedance. Capacitor impedance ($Z_C = \frac{1}{jC\omega}$) decreases at high frequency‡ while inductor impedance ($Z_L = jL\omega$) increases. Capacitor is then put across output voltage

*A reactive impedance is a purely imaginary impedance.

†Active filter allows to separate the filter parameters with those matching impedance.

‡angular frequency $\omega = 2\pi f$

and inductor between input and output voltage (Fig. 1.2) to perform low pass filtering.

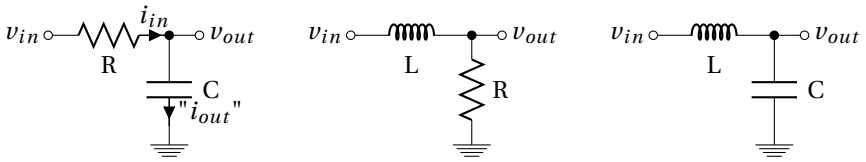


Figure 1.2: Passive low-pass filter : first order R-C, first order L-R and second order L-C.

Generalization : whatever impedances Z_x of the voltage bridge shown in figure 1.3, voltage transfer functions H are generalized as expression 1.1 by calculating the divider's voltage ratio using Kirchhoff's voltage law*.

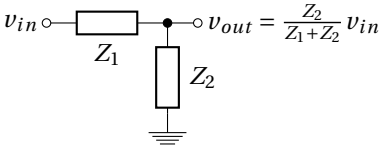


Figure 1.3: Impedance bridge voltage divider.

$$H(\omega) = \frac{v_{out}}{v_{in}} = \frac{Z_2}{Z_1 + Z_2} \tag{1.1}$$

Voltage transfer functions of filters given in figure 1.2 are then expressed as :

$$H_{RC} = \frac{Z_C}{R + Z_C} = \frac{\frac{1}{jC\omega}}{R + \frac{1}{jC\omega}} \quad \Longrightarrow \quad \boxed{H_{RC} = \frac{1}{1 + jRC\omega}} \tag{1.2}$$

$$\text{cut-off frequency} \equiv |H_{RC}| = \frac{1}{\sqrt{2}} \rightarrow RC\omega_c = 1 \rightarrow f_c\Big|_{RC} = \frac{1}{2\pi RC}$$

$$H_{LR} = \frac{R}{R + Z_L} = \frac{R}{R + jL\omega} \quad \Longrightarrow \quad \boxed{H_{LR} = \frac{1}{1 + j\frac{L}{R}\omega}} \tag{1.3}$$

$$f_c\Big|_{LR} = \frac{R}{2\pi L}$$

$$H_{LC} = \frac{Z_C}{Z_L + Z_C} = \frac{\frac{1}{jC\omega}}{jL\omega + \frac{1}{jC\omega}} \quad \Longrightarrow \quad \boxed{H_{LC} = \frac{1}{1 - LC\omega^2}} \tag{1.4}$$

$$f_0\Big|_{LC} = \frac{1}{2\pi\sqrt{LC}}$$

☞ A filter can also be used to **convert** a current to a voltage or a voltage to a current in addition to a simple filtering †. Considering for example the first R-C low-pass filter in figure 1.2. We can define

*The sum of the voltage sources in a closed loop is equivalent to the sum of the potential drops in that loop : $v_{in} = Z_1 \times \underbrace{\frac{v_{out}}{Z_2}}_{i_{in}="i_{out}"} + v_{out}$

†To filter a current, two impedances in parallel are require : current divider. In our example without load impedance $i_{in} = i_{out}$. Current transfer function $\frac{"i_{out}"}{i_{in}}$ is then always equal to 1.

trans-impedance transfer function $\frac{v_{out}}{i_{in}}$ and also **the trans-admittance transfer function** $\frac{"i_{out}"}{v_{in}}$:

$$\frac{v_{out}}{i_{in}} = \frac{v_{out}}{"i_{out}"} = Z_C = \frac{1}{jC\omega} \longrightarrow \text{Integrator} \tag{1.5}$$

$$\frac{"i_{out}"}{v_{in}} = \frac{1}{R+Z_C} = \frac{1}{R+\frac{1}{jC\omega}} = \frac{jC\omega}{1+jRC\omega} \longrightarrow \text{High-pass filter} \tag{1.6}$$

1.2.2 S plane (Laplace domain)

For transient analysis, filter transfer function H must be represented as a function of the complex number s :

$$s = \sigma + j\omega \tag{1.7}$$

Then, reactive impedances are expressed as function of this complex number :

$$Z_L = Ls \tag{1.8}$$

$$Z_C = \frac{1}{Cs} \tag{1.9}$$

Frequency response and stability information can be revealed by plotting in a complex plane (s plane) roots values of $H(s)$ numerator (zero) and denominator (pole).

- **Poles** are values of s such that transfer function $|H| \to \infty$,
- **Zeros** are values of s such that transfer function $|H| = 0$.

Considering the band-pass filter of the figure 1.4, the transfer function $H_{LCR} = \frac{v_{out}}{v_{in}}$ is given by equation 1.10.

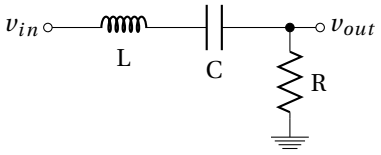


Figure 1.4: Passive band-pass LCR filter.

$$H_{LCR}(s) = \frac{R}{R+Ls+\frac{1}{Cs}} = \boxed{\frac{RCs}{1+RCs+LCs^2}} \tag{1.10}$$

The order of the filter (Fig. 1.4) is given by the degree of the denominator of the expression 1.10. A **zero** corresponds the numerator equal to zero. A **pole** is given by the denominator equal to zero. Each pole provides a -20dB/decade slope of the transfer function ; each zero a + 20 dB/decade [*]. Zero and pole can be real or complex. When they are complex, they have a conjugate pair [†].

Expression 1.10 is characterized by a zero at $s = 0$ and two conjugate poles obtained by nulling it's denominator (eq. 1.11)[‡].

$$0 = 1 + RCs + LCs^2 \xrightarrow[discri.]{} \Delta = (RC)^2 - 4LC \xrightarrow[roots]{} s_p = \frac{-RC \pm \sqrt{(RC)^2 - 4LC}}{2LC} \tag{1.11}$$

The discriminant Δ could be positive, null or negative as shown in figure 1.5. The boundary ($\Delta = 0$) between negative and positive discriminant is given by the equation $(RC)^2 = 4LC$ and could be rewrite $\frac{1}{2} = \frac{\sqrt{L/C}}{R}$ which is the expression of a parameter called the quality factor Q.

[*] $H[dB] = 20\log H[lin.]$ and a decade correspond to a variation by a factor of 10 in frequency. A times 10 ordinate increasing on a decade (times 10 abscissa increasing) correspond to a 20dB/decade slope on a logarithmic scale or also 6dB/octave. A -20dB/decade then correspond to a transfer function decreasing by a factor of 10 on a decade

[†] each conjugate pair has the same real part, but imaginary parts equal in magnitude and opposite in sign

[‡] The roots (zeros) of a polynomial of degree 2 (quadratic function) $ax^2 + bx + c = 0$ are $x = \frac{-b \pm \sqrt{\Delta}}{2a}$ where the discriminant is $\Delta = b^2 - 4ac$

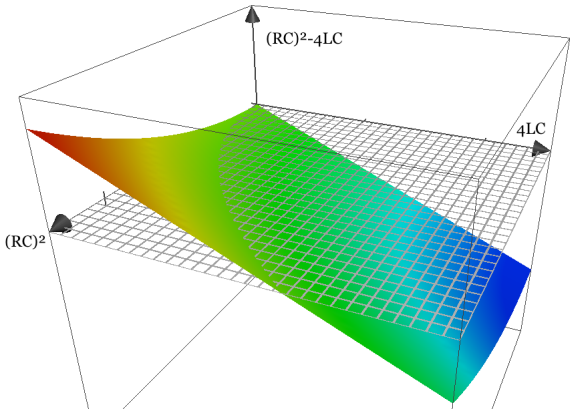


Figure 1.5: Discriminant $\Delta = (RC)^2 - 4LC$ value as function of $(RC)^2$ and $4LC$.

Nature (real or imaginary) of the roots is reported in the table 1.1.

$\Delta = (RC)^2 - 4LC$	roots s_p	$Q = \frac{\sqrt{L/C}}{R}$
> 0	2 real	$< 1/2$
$= 0$	1 real *double*	$= 1/2$
< 0	2 complex conjugates	$> 1/2$

Table 1.1: Link between discriminant sign and nature of the roots. Conditions on the R, L and C device values are reported expressed as the quality factor Q.

Roots are expressed as two complex conjugate roots [*] : the poles s_{p_1} and s_{p_2} given on 1.12.

$$\boxed{s_{p_{1,2}} = \frac{-R}{2L} \pm j\sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}} \tag{1.12}$$

The natural angular frequency ω_0 is the module of the pole :

$$\omega_0 = |s_{p_{1,2}}| = \frac{1}{\sqrt{LC}} \tag{1.13}$$

In a s plane, pole and zero allow to locate where the magnitude of the transfer function is large (near pole), and where it is small (near zero). This provides us understanding of what the filter does at different frequencies and is used to study the stability. Figure 1.6 shows pole (✖) and zero (●) in a s plane.

A causal linear system is stable if real part of all poles is negative. On the s plane, this corresponds to a pole localization at the left side (Fig. 1.7).

☞ *Laplace notation $s = \sigma + j\omega$ is required to study stability condition and transient (time domain) analysis. However, for steady state signal (frequency domain) analysis, Fourier notation $s = j\omega$ is preferred to do harmonic analysis.*

1.2.3 Bode plot (Fourier domain)

The most common way to represent the transfer function of a filter is the Bode plot. Bode plot is usually a combination of the magnitude $|H|$ and the phase ϕ of the transfer function on a log frequency axis.

[*] $\sqrt{x}|_{x<0} = i\sqrt{|x|}$

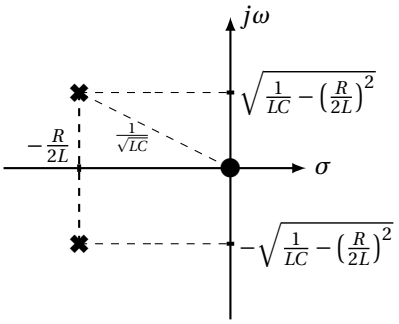


Figure 1.6: Pole (✖) and zero (●) representation of the RLC filter (Fig. 1.4) into the *s* plane.

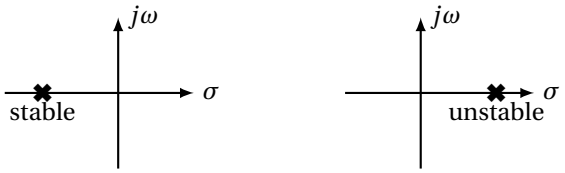


Figure 1.7: Stable if all poles are in the left hand *s* plane (*i.e.* have negative real parts).

Using the LCR band-pass filter (figure 1.4 example), the magnitude* and the phase† of the expression 1.10 (rewrite with unity numerator in 1.14) are respectively given by expressions 1.15 and 1.16. To do this, Fourier transform is used (harmonic regime) instead of Laplace transform : **s is replaced by j**ω, only.

$$H_{LCR} = \frac{jRC\omega}{1 + jRC\omega - LC\omega^2} = \frac{1}{1 + j\left(\frac{L\omega}{R} - \frac{1}{RC\omega}\right)} \tag{1.14}$$

$$|H_{LCR}| = \frac{1}{\sqrt{1 + \left(\frac{L\omega}{R} - \frac{1}{RC\omega}\right)^2}} \tag{1.15}$$

$$\phi_{LCR} = \arg(H_{LCR}) = -\arctan\left(\frac{L\omega}{R} - \frac{1}{RC\omega}\right) \tag{1.16}$$

Numerical Application : L = 1 mH, C = 100 nF and R = 100 Ω

- The natural ‡ frequency $f_0 = \frac{1}{2\pi\sqrt{LC}} = \frac{10^5}{2\pi} \approx 16\ kHz$

The band-pass filter could be seen as a cascading high and a low-pass filter :

- The high pass-filter cutoff frequency $f_{c1} = \frac{R}{2\pi L}$
- The low pass-filter cutoff frequency $f_{c2} = \frac{1}{2\pi RC}$

The Bode diagram of this band-pass filter is plotted on figure 1.8.

☞ With this specific numerical application $f_0 = f_{c1} = f_{c2}$. f_0, f_{c1} and f_{c2} are however not necessarily equal. Nevertheless, whatever the numerical application, $\boxed{f_0 = \sqrt{f_{c1} f_{c2}}}$

*Absolute value or module

†Argument

‡In the case of band-pass filter, *natural frequency* is also called *resonance frequency* or *center frequency* corresponding to $LC\omega_0^2 = 1$. This is the frequency at which the impedance of the circuit is purely resistive.

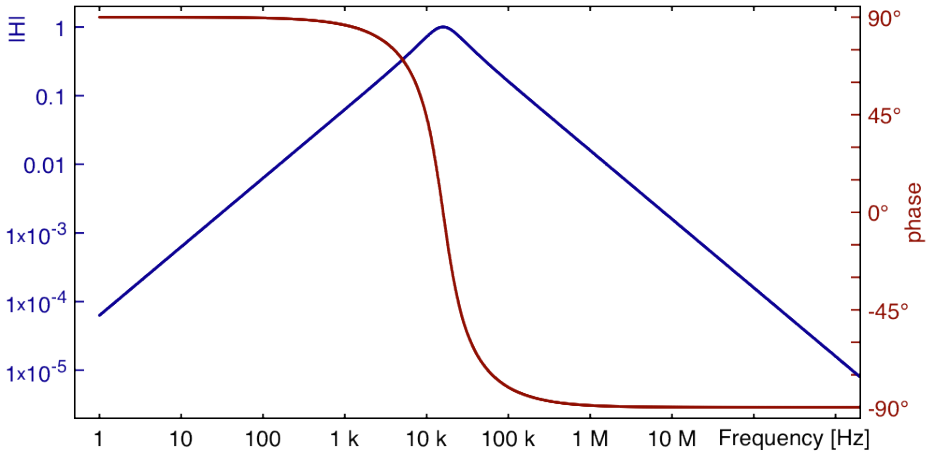


Figure 1.8: Bode plot of the LCR band-pass filter figure 1.4.

In this numerical application $f_0 = f_{c1} = f_{c2}$ (Fig 1.8). This correspond to a particular case where the quality factor $Q = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{1}{100}\sqrt{\frac{10^{-3}}{10^{-7}}} = 1$. For other numerical application (i.e. $Q \neq 1$), f_0 is different than f_{c1} and f_{c2} (Fig 1.9).

Quality factor Q

Quality factor Q is a dimensionless parameter which indicates how much is the sharpness of a multi-pole filter response around its cut-off (or center *) frequency. In the case of a band-pass filter, its expression 1.17 is the ratio of the center frequency by the -3 dB bandwidth $(BW)^\dagger$ and is given for series and parallel LCR circuit.

$$\begin{aligned} Q = \frac{f_0}{BW} &= \frac{f_{c2}}{f_{c1}}\Big|_{\text{band-pass filter}} \\ &= \frac{1}{R}\sqrt{\frac{L}{C}}\Big|_{\text{series LCR}} \\ &= R\sqrt{\frac{C}{L}}\Big|_{\text{parallel LCR}} \end{aligned} \tag{1.17}$$

Quality factor is directly proportional to the **selectivity** of a band-pass filter (Fig. 1.9) :

- Q < $\frac{1}{2}$ → damped and wide band filter
- Q = $\frac{1}{2}$ → critically damped
- Q > $\frac{1}{2}$ → resonant and narrow band filter

We have already see that $Q = 1/2$ is related to the denominator roots of the transfer function, see table 1.1.

In practice, Q factor is proportional to the ratio between the maximum energy stored in the reactive devices and the energy losses in the resistor :

$$Q = \omega_0 \frac{\text{Max. Energy Stored}}{\text{Power loss}} \tag{1.18}$$

*for a band-pass filter

† ⚠ For resonant circuits, $BW|_{@-3dB} \neq f_{c2} - f_{c1}$. Indeed, for $Q = 1$, $f_{c2} = f_{c1} = f_0$, but $BW = f_0$

The maximum stored energy is $LI^2_{L_{RMS}}$ or $CV^2_{C_{RMS}}$; the dissipated power is $RI^2_{R_{RMS}}$ or $\frac{V^2_{R_{RMS}}}{R}$ and $\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{LC}}$. In series LCR, $I_L = I_C = I_R$. In parallel LCR, $V_L = V_C = V_R$. So, it is easy to link equations 1.17 and 1.18.

We can again rewrite expression 1.14 by using now natural frequency f_0 and quality factor Q :

$$H_{LCR} = \frac{jRC\omega}{1 + jRC\omega - LC\omega^2} = \frac{j\frac{1}{Q}\frac{\omega}{\omega_0}}{1 + j\frac{1}{Q}\frac{\omega}{\omega_0} - \frac{\omega^2}{\omega_0^2}} = \frac{j\frac{1}{Q}\frac{f}{f_0}}{1 + j\frac{1}{Q}\frac{f}{f_0} - \frac{f^2}{f_0^2}} = \frac{1}{1 + jQ\left(\frac{f}{f_0} - \frac{f_0}{f}\right)} \tag{1.19}$$

with $RC = \frac{1}{Q}\frac{1}{\omega_0}$, $Q = \frac{1}{R}\sqrt{\frac{L}{C}}$, $\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{LC}}$ and $\omega = 2\pi f$.

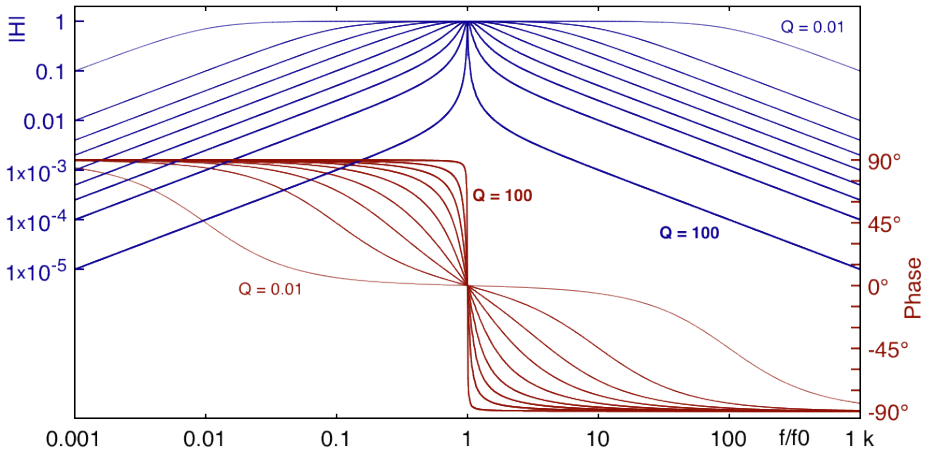


Figure 1.9: Bode plot of a band-pass filter - Q = 0.01 ; 0.1 ; 0.25 ; 0.5 ; 1 ; 2 ; 4 ; 10 ; 100 (*i.e.* ζ = 50 ; 5 ; 2 ; 1 ; 0.5 ; 0.25 ; 0.125 ; 0.05 ; 0.005).

Damping ratio ζ

Damping ratio ζ is generally used in the case of low and hight-pass filter (Low Q) when Q is used in the case of narrow band-pass filter, resonator and oscillator (High Q).

$$\zeta = \frac{1}{2Q} \tag{1.20}$$

The more damping the filter, the flatter its response is and likewise, the less damping the filter, the sharper its response is :

- $\zeta < 1$ → steep cutoff
- $\zeta = 1/\sqrt{2} = Q$ → -3dB attenuation at f_c (as for 1^{st} order)
- $\zeta = 1$ → critical damping
- $\zeta > 1$ → slow cutoff

Expression 1.14 may now be rewritten using damping factor :

$$H_{LCR} = \frac{jRC\omega}{1 + jRC\omega - LC\omega^2} = \frac{j2\zeta\frac{\omega}{\omega_0}}{1 + j2\zeta\frac{\omega}{\omega_0} - \frac{\omega^2}{\omega_0^2}} \tag{1.21}$$

1.3 Cascading filter stages

Circuit analysis by applying Kirchhoff's laws (as before) is usually used for first and second order filter. For a higher order filters, network synthesis approach may be used. A polynomial equation expresses the filtering requirement. Each first and second order filter elements are then defined from continued-fraction expansion of the polynomial expression. In practice, to avoid saturation, highest Q stage is placed at the end of the network.

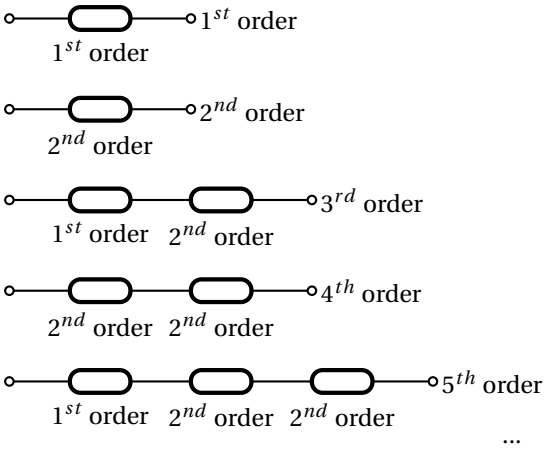


Figure 1.10: Cascading filter stages for higher-order filters.

It exists different type of polynomial equations from which the filter is mathematically derived. These type of filters are Butterworth, Bessel, Chebyshev, inverse Chebyshev, elliptic Cauer, Bessel, optimum Legendre, etc.

- **Butterworth** filter is known as the maximally-flat filter as regards to the flatness in the pass-band. The attenuation is simply -3 dB at the cutoff frequency ; above, the slope is -20dB/dec per order (n).

- **Chebychev** filter has a steeper rolloff* just after the cutoff frequency but ripple in the pass-band. The cutoff frequency is defined as the frequency at which the response falls below the ripple band †. For a given filter order, a steeper cutoff can be achieved by allowing more ripple in the pass-band (Chebyshev filter transient response shows overshoots).

- **Bessel** filter is characterized by linear phase response. A constant-group delay is obtained at the expense of pass-band flatness and steep rolloff. The attenuation is -3 dB at the cutoff frequency.

- **elliptic Cauer** (non-polynomials) filter has a very fast transition between the pass-band and the stop-band. But it has ripple behavior in both the passband and the stop-band (not studied after).

- **inverse Chebychev - Type II** filter is not as steeper rolloff than Chebychev but it has no ripple in the passband but in the stop band (not studied after).

- **optimum Legendre** filter is a tradeoff between moderate rolloff of the Butterworth filter and ripple in the pass-band of the Chebyshev filter. Legendre filter exhibits the maximum possible rolloff consistent with monotonic magnitude response in the pass-band.

*rolloff = transition from the pass band to the stop band.

†The cutoff frequency of a Tchebyshev filter is not necessarily defined at - 3dB. f_c is the frequency value at which the filter transfer function is equal to $\frac{1}{\sqrt{1+\epsilon^2}}$ but continues to drop into the stop band. ϵ is the ripple factor. Chebyshev filter is currently given for a given ϵ ($20\log\sqrt{1+\epsilon}$) in [dB].

1.3.1 Polynomial equations

Filters are syntheses by using a H_0 DC gain and a polynomial equations P_n, with n the order of the equation, and so, of the filter. The transfer function of a synthesized low-pass filter is $H(s) = \frac{H_0}{P_n\left(\frac{s}{\omega_c}\right)}$ with ω_c the cutoff angular frequency and $s = j\omega \Big|_{\text{Fourier domain}} = \sigma + j\omega \Big|_{\text{Laplace domain}}$.

Butterworth polynomials

Butterworth polynomials are obtained by using expression 1.22 :

$$P_n(\omega) = B_n(\omega) = \sqrt{1 + \left(\frac{\omega}{\omega_c}\right)^{2n}} \tag{1.22}$$

The roots* of these polynomials occur on a circle of radius ω_c at equally spaced points in the s plane :

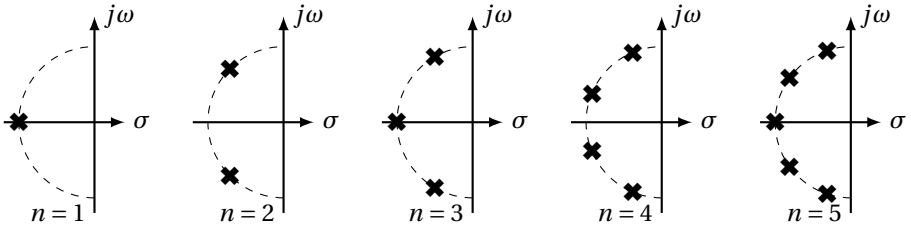


Figure 1.11: Pole locations of 1^{st}, 2^{nd}, 3^{rd}, 4^{th} and 5^{th} order Butterworth filter.

Poles of a $H(s)H(-s) = \frac{H_0^2}{1+\left(\frac{-s^2}{\omega_c^2}\right)^n}$ low pass filter transfer function module are specified by :

$$\frac{-s_x^2}{\omega_c^2} = (-1)^{\frac{1}{n}} = e^{j\frac{(2x-1)\pi}{n}} \quad \text{with} \quad x = 1,2,3,\ldots,n \tag{1.23}$$

The denominator of the transfer function may be factorized as :

$$H(s) = \frac{H_0}{\prod_{x=1}^{n} \frac{s-s_x}{\omega_c}} \tag{1.24}$$

The denominator of equation 1.24 is a Butterworth polynomial in s. Butterworth polynomials are usually expressed with real coefficients by multiplying conjugate poles †. The normalized‡ Butterworth polynomials has the form :

$$\begin{aligned} B_0 &= 1 \\ B_1 &= s+1 \\ B_n &= \prod_{x=1}^{\frac{n}{2}} \left[s^2 - 2s\,cos\left(\frac{2x+n-1}{2n}\pi\right) + 1 \right] \qquad \text{n is even} \\ &= (s+1) \prod_{x=1}^{\frac{n-1}{2}} \left[s^2 - 2s\,cos\left(\frac{2x+n-1}{2n}\pi\right) + 1 \right] \qquad \text{n is odd} \end{aligned} \tag{1.25}$$

☞ Second order Butterworth filter correspond to the particular case where $Q = \zeta = 1/\sqrt{2} \approx 0.71$. Indeed, from equation 1.25 and expressing the Butterworth polynomial as the denominator of the equation 1.19, it is easy to determined for $n = 2$ that : $\frac{1}{Q} = 2cos\left(\underbrace{\frac{2+2-1}{2\times 2}\pi}_{3\pi/4}\right) = \sqrt{2} \approx 1.41$ with $Q = \frac{1}{2\zeta}$ (Eq. 1.20).

*Roots of B_n are poles of the low-pass filter transfer function $H(s)$.

†for example s_1 and s_n are complex conjugates

‡normalized : $\omega_c = 1$ and $H_0 = 1$

Chebyshev polynomials

Chebyshev polynomials are obtained by using expression 1.26 :

$$P_n = T_n = \begin{cases} \cos(n \arccos(\omega)) & |\omega| \leq 1 \\ \cosh(n \operatorname{arcosh}(\omega)) & |\omega| \geq 1 \end{cases} \tag{1.26}$$

where the hyperbolic cosine function $\cosh(x) = \cos(jx) = \frac{e^x + e^{-x}}{2}$. From the two first values $T_0 = 1$ and $T_1 = \omega$, Chebyshev polynomials $T_n(\omega)$ could be recursively obtained by using expression 1.27 :

$$\begin{aligned} &T_0 = 1 \\ &T_1 = \omega \\ &T_n = 2\omega T_{n-1} - T_{n-2} \begin{cases} T_2 = 2\omega^2 - 1 \\ T_3 = 4\omega^3 - 3\omega \\ T_4 = 8\omega^4 - 8\omega^2 + 1 \\ \dots \end{cases} \end{aligned} \tag{1.27}$$

Chebyshev low-pass filter frequency response is generally obtained by using a slightly more complex expression than for a Butterworth one :

$$|H(s)| = \frac{H_0'}{\sqrt{1 + \epsilon^2 T_n^2\left(\frac{\omega}{\omega_c}\right)}} \tag{1.28}$$

where ϵ is the ripple factor [*]. Even if $H_0' = 1$, magnitude of a Chebyshev low-pass filter is not necessarily equal to 1 at low frequency ($\omega = 0$). Gain will alternate between maxima at 1 and minima at $\frac{1}{\sqrt{1+\epsilon^2}}$.

$$T_n\left(\frac{\omega}{\omega_c} = 0\right) = \begin{cases} \pm 1 & n \text{ is even} \\ 0 & n \text{ is odd} \end{cases} \quad \Rightarrow \quad H\left(\frac{\omega}{\omega_c} = 0\right) = \begin{cases} \frac{1}{\sqrt{1+\epsilon^2}} & n \text{ is even} \\ 1 & n \text{ is odd} \end{cases} \tag{1.29}$$

At the cutoff angular frequency ω_c, the gain is also equal to $\frac{1}{\sqrt{1+\epsilon^2}}$ (but $\forall n$) and, as the frequency increases, it drops into the stop band.

$$T_n\left(\frac{\omega}{\omega_c} = 1\right) = \pm 1 \quad \forall n \quad \Rightarrow \quad H\left(\frac{\omega}{\omega_c} = 1\right) = \pm \frac{1}{\sqrt{1+\epsilon^2}} \quad \forall n \tag{1.30}$$

Finally, conjugate poles s_x (equation 1.31 [†]) of expression 1.28 are obtained by solving equation $0 = 1 + \epsilon^2 T_n^2$:

$$s_x = \sin\left(\frac{2x-1}{n}\frac{1}{2\pi}\right)\sinh\left(\frac{1}{n}\operatorname{arcsinh}\frac{1}{\epsilon}\right) + j\cos\left(\frac{2x-1}{n}\frac{1}{2\pi}\right)\cosh\left(\frac{1}{n}\operatorname{arcsinh}\frac{1}{\epsilon}\right) \tag{1.31}$$

Using poles, transfer function of a Chebyshev low-pass filter is rewritten as equation 1.28 :

$$H(s) = \begin{cases} \frac{\frac{1}{\sqrt{1+\epsilon^2}}}{\prod_{x=1}^{n} \frac{s - s_x}{\omega_c}} & n \text{ is even} \\ \frac{1}{\prod_{x=1}^{n} \frac{s - s_x}{\omega_c}} & n \text{ is odd} \end{cases} \tag{1.32}$$

[*] $\epsilon = 1$ for the other polynomials filter and is then not represented

[†] Poles are located on a centered ellipse in s plane ; with real axis of length $\sinh\left(\frac{1}{n}\operatorname{arcsinh}\frac{1}{\epsilon}\right)$ and imaginary axis of length $\cosh\left(\frac{1}{n}\operatorname{arcsinh}\frac{1}{\epsilon}\right)$.

Bessel polynomials

Bessel polynomials are obtained by using expression 1.33 :

$$P_n = \theta_n = \sum_{x=0}^{n} s^x \frac{(2n-x)!}{2^{n-x}x!(n-x)!} \begin{cases} \theta_1 = s+1 \\ \theta_2 = s^2+3s+3 \\ \theta_3 = s^3+6s^2+15s+15 \\ \dots \end{cases} \tag{1.33}$$

Bessel low-pass filter frequency response is given by expression 1.34 and is also given for n = 2 (delay normalized second-order Bessel low-pass filter).

$$\frac{\theta_n(0)}{\theta_n\left(\frac{s}{\omega_c}\right)} \quad \Longrightarrow \quad n=2 \quad \frac{3}{\left(\frac{s}{\omega_c}\right)^2+3\frac{s}{\omega_c}+3} = \frac{1}{\frac{1}{3}\left(\frac{s}{\omega_c}\right)^2+\frac{s}{\omega_c}+1} \tag{1.34}$$

However, Bessel polynomials θ_n have been normalized to unit delay at $\frac{\omega}{\omega_c}=0$ (delay normalized) and are not directly usable for classical cutoff frequency at -3 dB standard (frequency normalized).

To compare this polynomials to the other one, the table 1.2 gives BCF factors for converting Bessel filter parameters to **3 dB attenuation at** $\frac{\omega}{\omega_c}=1$. These factors were used in preparing the frequency normalized tables given on Appendix I.

n	BCF
2	1.3616
3	1.7557
4	2.1139
5	2.4274
6	2.7034
7	2.9517
8	3.1796
9	3.3917

Table 1.2: Bessel conversion factor - BCF

By using BCF factor and for n = 2 we finally see in expression 1.35 the frequency response of a second order Bessel low pass filter :

$$H_2 = \frac{1}{\frac{BCF^2}{3}\left(\frac{s}{\omega_c}\right)^2+BCF\frac{s}{\omega_c}+1} \approx \frac{1}{0.618\left(\frac{s}{\omega_c}\right)^2+1.3616\frac{s}{\omega_c}+1} \tag{1.35}$$

Module and phase are deduced from the equation 1.35 :

$$\begin{aligned} |H_2| &= \frac{1}{\sqrt{\left(1-0.618\frac{\omega^2}{\omega_c^2}\right)^2+\left(1.3616\frac{\omega}{\omega_c}\right)^2}} \\ \phi &= \arg(H_2) = -\arctan\left(\frac{1.3616\frac{\omega}{\omega_c}}{1-0.618\frac{\omega^2}{\omega_c^2}}\right) \end{aligned} \tag{1.36}$$

Bessel filter is characterized by a linear phase response. Group delay could be studied by calculating :

$$\tau_g = -\frac{d\phi}{d\omega} \tag{1.37}$$

Legendre polynomials

From the two first values $P_0(x)=1$ and $P_1(x)=x$, (as for Chebyshev) Legendre polynomials $P_n(\omega^2)$ could be recursively obtained by using expression 1.38 :

$$
\begin{aligned}
&P_0(x) = 1\\
&P_1(x) = x\\
&P_{n+1}(x) = \frac{(2n+1)xP_n(x) - nP_{n-1}(x)}{n+1}
\begin{cases}
P_2(x) &= \frac{3x^2}{2} - \frac{1}{2}\\
P_3(x) &= \frac{5x^3}{2} - \frac{3x}{2}\\
P_4(x) &= \frac{35x^4}{8} - \frac{30x^2}{8} + \frac{3}{8}\\
\dots
\end{cases}
\end{aligned}
\tag{1.38}
$$

From these polynomials, Legendre low-pass filter (expression 1.39) also called optimal filter are not directly defined from P_n but from optimal polynomials $L_n(\omega^2)$ described on expressions 1.40.

$$
H(\omega) = \frac{1}{\sqrt{1 + L_n(\omega^2)}}
\tag{1.39}
$$

$$
L_n(\omega^2) = \begin{cases}
\int_{-1}^{2\omega^2-1} \left(\sum_{i=0}^{k} a_i P_i(x)\right)^2 dx & n = 2k+1 \text{ is odd}\\
\int_{-1}^{2\omega^2-1} (x+1)\left(\sum_{i=0}^{k} a_i P_i(x)\right)^2 dx & n = 2k+2 \text{ is even}
\end{cases}
$$

$$
\text{with } a_i \begin{cases}
n \text{ is odd} \quad \forall k & a_0 = \frac{a_1}{3} = \frac{a_2}{5} = \dots = \frac{a_i}{2i+1} = \frac{1}{\sqrt{2}(k+1)}\\
n \text{ is even} \begin{cases}
k \text{ is odd} & \begin{cases} \frac{a_1}{3} = \frac{a_3}{7} = \frac{a_5}{11} = \dots = \frac{a_i}{2i+1} = \frac{1}{\sqrt{2}(k+1)(k+2)} \\ a_0 = a_2 = a_4 = \dots = a_i = 0 \end{cases}\\
k \text{ is even} & \begin{cases} a_0 = \frac{a_2}{5} = \frac{a_4}{9} = \dots = \frac{a_i}{2i+1} = \frac{1}{\sqrt{2}(k+1)(k+2)} \\ a_1 = a_3 = a_5 = \dots = a_{i-1} = 0 \end{cases}
\end{cases}
\end{cases}
\tag{1.40}
$$

Finally, optimal polynomials could be calculated :

$$
\begin{aligned}
&L_0(\omega^2) = 1\\
&L_1(\omega^2) = \omega^2\\
&L_2(\omega^2) = \omega^4\\
&L_3(\omega^2) = \omega^2 - 3\omega^4 + 3\omega^6\\
&L_4(\omega^2) = 3\omega^4 - 8\omega^6 + 6\omega^8\\
&L_5(\omega^2) = \omega^2 - 8\omega^8 + 28\omega^6 - 40\omega^8 + 20\omega^{10}\\
&\quad \dots
\end{aligned}
\tag{1.41}
$$

Factorization of the overall attenuation function* $\sqrt{1 + L_n(\omega^2)}$ is given on Appendix I.

☞ *However, it is not so important* † *to know how found Butterworth, Chebyshev, Bessel or Legendre polynomials coefficients; but it is more useful to know how to use them to design efficient filters. This is why it exists a lot of filter tables to simplify circuit design based on the idea of* **cascading lower order stages to realize higher-order filters.**

1.3.2 Filter Tables

Filter tables could give complex roots or normalized polynomials coefficients c_0, c_1, …, c_n with $P_n = c_n s^n + c_{n-1} s^{n-1} + \dots + c_1 s + c_0$. However, more currently filter tables show factorized polynomials or directly normalized cutoff frequency (Scaling Factor - SF) and quality factor (Q) of each of stages for the particular filter being designed.

☞ *Some tables are now given using a Butterworth low-pass filter example.*

*Attenuation function = denominator of a low pass filter

†for a filter designer point of view

Roots table

Some filter tables give complex roots of polynomials. Table 1.3 shows roots of Butterworth polynomials (they are obtained by using equation 1.25).

order n	σ	$j\omega$
1	-1	0
2	-0.7071	±0.7071
3	-0.5	±0.866
	-1	0
4	-0.3827	±0.9239
	-0.9239	±0.3827
5	-0.309	±0.951
	-0.809	±0.5878
	-1	0
6	-0.2588	±0.9659
	-0.7071	±0.7071
	-0.9659	±0.2588
7	-0.2225	±0.9749
	-0.6235	±0.7818
	-0.901	±0.4339
	-1	0
8	-0.1951	±0.9808
	-0.5556	±0.8315
	-0.8315	±0.5556
	-0.9808	±0.1951
9	-0.1736	±0.9848
	-0.5	±0.866
	-0.766	±0.6428
	-0.9397	±0.342
	-1	0

Table 1.3: Butterworth polynomials complex roots.

This table is also an indication of pole locations (in s plane) of low-pass filter having Butterworth polynomials as a transfer function denominator. Notice that σ is always negative (stability condition).

Polynomials coefficients table

An other table, concerning polynomials, shows directly coefficients c_x of polynomials as shown in table 1.4 for Butterworth polynomials $P_n = B_n = \sum_{x=0}^{n} c_x s^x = c_n s^n + c_{n-1} s^{n-1} + \cdots + c_1 s + c_0$.

n	c_0	c_1	c_2	c_3	c_4	c_5	c_6	c_7	c_8	c_9	c_{10}
1	1	1									
2	1	1.41	1								
3	1	2	2	1							
4	1	2.61	3.41	2.61	1						
5	1	3.24	5.24	5.24	3.24	1					
6	1	3.86	7.46	9.14	7.46	3.86	1				
7	1	4.49	10.1	14.59	14.59	10.1	4.49	1			
8	1	5.13	13.14	21.85	25.69	21.85	13.14	5.13	1		
9	1	5.76	16.58	31.16	41.99	41.99	31.16	16.58	5.76	1	
10	1	6.39	20.43	42.8	64.88	74.23	64.88	42.8	20.43	6.39	1

Table 1.4: Butterworth polynomials coefficients c_x. $P_n = B_n = \sum_{x=0}^{n} c_x s^x = c_n s^n + c_{n-1} s^{n-1} + \cdots + c_1 s + c_0$.

However, polynomials are generally factored in terms of 1^{st} and 2^{nd} order polynomials ; particularly to build cascading 1^{st} and 2^{nd} order filters.

Factored polynomials table

To cascade 1^{st} and 2^{nd} order filters (filter synthesis), a more useful table gives a **factored representation of polynomials** as the Butterworth quadratic factors in Table 1.5.

n	$P_n = B_n$
1	$s+1$
2	$s^2+1.4142s+1$
3	$(s+1)(s^2+s+1)$
4	$(s^2+0.7654s+1)(s^2+1.8478s+1)$
5	$(s+1)(s^2+0.618s+1)(s^2+1.618s+1)$
6	$(s^2+0.5176s+1)(s^2+1.4142s+1)(s^2+1.9319s+1)$
7	$(s+1)(s^2+0.445s+1)(s^2+1.247s+1)(s^2+1.8019s+1)$
8	$(s^2+0.3902s+1)(s^2+1.1111s+1)(s^2+1.6629s+1)(s^2+1.9616s+1)$
9	$(s+1)(s^2+0.3473s+1)(s^2+s+1)(s^2+1.5321s+1)(s^2+1.8794s+1)$
10	$(s^2+0.3129s+1)(s^2+0.908s+1)(s^2+1.4142s+1)(s^2+1.782s+1)(s^2+1.9754s+1)$

Table 1.5: Butterworth polynomials quadratic factors.

Cutoff frequencies and quality factor table

Finally, an other useful table for filter designer is table which gives directly cutoff frequency and quality factor of each 2^{nd} order filter. Table 1.6 gives frequency scaling factor and quality factor of Butterworth low-pass filter. A first order stage is just defined by a normalized cutoff frequency (SF) without quality factor (Q). Scaling factor is the ratio between the cutoff frequency of the considering stage and the cutoff frequency of the overall cascaded filter. So, finally the polynomial is expressed as in equation 1.42.

$$2^{nd}\text{order polynomial form} \rightarrow \boxed{P_n = 1 + j\frac{1}{Q}\frac{f}{SF f_c} - \left(\frac{f}{SF f_c}\right)^2} \tag{1.42}$$

☞ *In the particular case of Butterworth filter, the frequency scaling factor (SF) is always equal to one**.

order n	1^{st} stage		2^{nd} stage		3^{rd} stage		4^{th} stage		5^{th} stage	
	SF	Q	SF	Q	SF	Q	SF	Q	SF	Q
1	1									
2	1	0.7071								
3	1	1	1							
4	1	0.5412	1	1.3065						
5	1	0.618	1	1.6181	1					
6	1	0.5177	1	0.7071	1	1.9320				
7	1	0.5549	1	0.8019	1	2.2472	1			
8	1	0.5098	1	0.6013	1	0.8999	1	2.5628		
9	1	0.5321	1	0.6527	1	1	1	2.8802	1	
10	1	0.5062	1	0.5612	1	0.7071	1	1.1013	1	3.1969

Table 1.6: Butterworth normalized cutoff frequency (Scaling Factor - SF) and quality factor (Q) for each stages.

1.3.3 The use of filter tables

To build, for example, a **second order Butterworth low-pass filter** we need to do the transfer function $H(s) = \frac{H_0}{P_n\left(\frac{s}{\omega c}\right)}$ where P_n is a second order Butterwoth polynomials *i.e.* $P_n = B_2$.

*each 1^{st} and 2^{nd} order filter have the same cutoff frequency than the Butterworth cascading filter has at the end. This is not the case for other polynomials filter as Chebyshev for which SF is often different than 1.

Table 1.3 could be used to write $B_2 = \left(\frac{s}{\omega_c} - r_1\right)\left(\frac{s}{\omega_c} - r_1^*\right)$ with r_1 and r_1^* the two conjugate roots $-0.7071 \pm j0.7071$. The transfer function of the Butterworth low-pass filter could be expressed as equation 1.43.

$$H(s) = \frac{H_0}{B_2\left(\frac{s}{\omega_c}\right)} = \frac{H_0}{\left(\frac{s}{\omega_c} + 0.7071 - j0.7071\right)\left(\frac{s}{\omega_c} + 0.7071 + j0.7071\right)} \tag{1.43}$$

The denominator development of the expression 1.43 gives a quadratic form (expression 1.44) which clearly shows Butterworth polynomial coefficients given on table 1.4 and quadratic factors of table 1.5. It is also clear that expression 1.44 is similar to a classical representation of a transfer function with quality factor where SF and Q are finally what we can directly obtain from the table 1.6.

$$H(s) = \frac{H_0}{\left(\frac{s}{\omega_c}\right)^2 + 1.41\frac{s}{\omega_c} + 1} = \frac{H_0}{1 + j\frac{1}{Q}\frac{f}{SF f_c} - \frac{f^2}{SF^2 f_c^2}} \quad \text{with} \quad \begin{cases} SF = 1 \\ Q \approx \frac{1}{1.41} \approx 0.7071 \end{cases} \tag{1.44}$$

Bode diagram of this low pass filter could be expressed as equation 1.45 and plotted as figure 1.12.

$$\begin{aligned} |H(\omega)| &= \frac{1}{\sqrt{\left[1 - \left(\frac{\omega}{\omega_c}\right)^2\right]^2 + \left(1.41\frac{\omega}{\omega_c}\right)^2}} \quad \text{with} \quad H_0 = 1 \\ \phi(\omega) = \arg(H) &= -\arctan\frac{1.41\frac{\omega}{\omega_c}}{1 - \left(\frac{\omega}{\omega_c}\right)^2} \end{aligned} \tag{1.45}$$

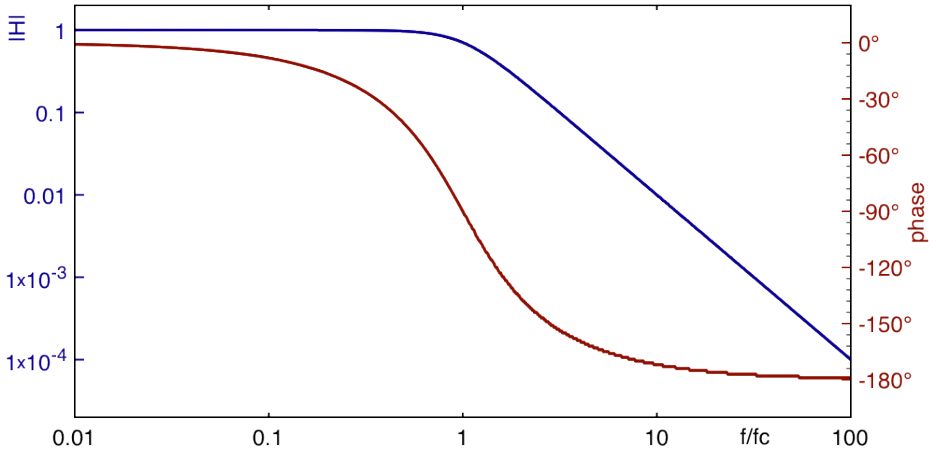


Figure 1.12: Bode plot of a second order Butterworth low-pass filter.

1.3.4 Conversion from low-pass filter

Low-pass to high-pass filter Filter tables give polynomials for low and high-pass filter. To obtain a high pass filter, a first order low pass filter transfer function $\frac{H_0}{c_0 + c_1 s}$ becomes $\frac{H_\infty s}{c_1 + c_0 s}$; and a second order low pass filter transfer function $\frac{H_0}{c_0 + c_1 s + c_2 s^2}$ becomes $\frac{H_\infty s^2}{c_2 + c_1 s + c_0 s^2}$. Figure 1.13 shows low and high pass filter with H_0 and H_∞ [*].

[*] In practice, there is always a frequency limitation which leads to a low-pass filtering. Consequently, an ideal high-pass filter never exists and $H_\infty \to 0$. So, in the case of real high pass filter, H_∞ corresponds more to the gain just after the cut-off frequency than that at infinity.

$$\begin{aligned} H_{LP_1} &= \frac{H_0}{c_0 + c_1 s} \quad \Rightarrow \quad H_{HP_1} = \frac{H_\infty}{c_0 + c_1/s} \\ H_{LP_2} &= \frac{H_0}{c_0 + c_1 s + c_2 s^2} \quad \Rightarrow \quad H_{HP_2} = \frac{H_\infty}{c_0 + c_1/s + c_2/s^2} \end{aligned} \tag{1.46}$$

Low to high pass filter conversion: $s \Rightarrow s^{-1}$

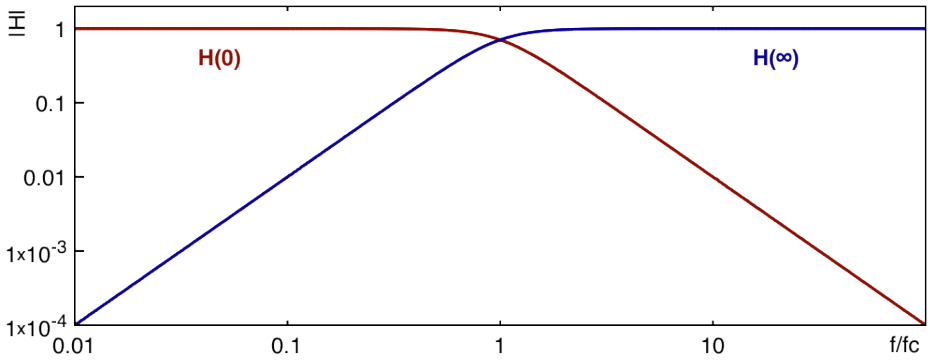


Figure 1.13: H_0 the low frequency gain of a low-pass filter and H_∞ the high frequency gain of a high-pass filter.

Band-pass filter For band-pass filter, it exists specific tables which give specific coefficients given for different bandwidth (BW). However, a low pass filter transfer function could be converted in band-pass filter by replacing s by $\frac{f_0}{BW}\left(s + s^{-1}\right)$; where $\frac{f_0}{BW}$ is equal to the quality factor Q.

Low to band-pass filter conversion: $s \Rightarrow Q\left(s + s^{-1}\right)$

Band-reject filter A low pass filter transfer function is converted in band-reject filter by replacing s by $\frac{1}{\frac{f_0}{BW}\left(s+s^{-1}\right)}$.

Low to band-reject filter conversion: $s \Rightarrow Q^{-1}\left(s + s^{-1}\right)^{-1}$

Transposition A synthesis of different transpositions are reported in the table 1.7.

Conv. \ Filter type	Low-pass	High-pass	Band-pass	Band-reject
Normalized complex frequency	s	s^{-1}	$Q\left(s + s^{-1}\right)$	$\frac{1}{Q}\frac{1}{s+s^{-1}}$
First order transfert function	$\frac{1}{C_0+C_1 s}$	$\frac{1}{C_0+C_1/s}$	$\frac{1}{C_0+C_1 Q(s+s^{-1})}$	$\frac{1}{C_0+\frac{C_1}{Q(s+s^{-1})}}$
Second order transfert function	$\frac{1}{C_0+C_1 s+C_2 s^2}$	$\frac{1}{C_0+C_1/s+C_2/s^2}$		

Table 1.7: Filter normalized transposition.

☞ *The transfer function is obtained by using filter table after determination of type and order. The next step is to determine a circuit to implement these filters.*

1.4 Filter synthesis

It exists different topologies of filter available for filter synthesis. The most often used topology for an active realization is Sallen-Key topology (Fig. 1.14).

1.4.1 Sallen-Key topology

Sallen-Key electronic circuit (Fig. 1.14) is used to implement second order active filter.

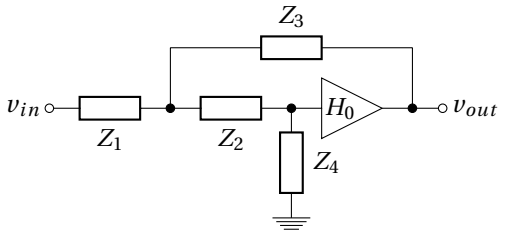


Figure 1.14: Sallen-Key generic topology.

From Kirchhoff laws, transfer function of the generic Sallen-Key topology could be written as :

$$H_{SK} = \frac{H_0}{1 + \left[\frac{Z_1+Z_2}{Z_4} + (1-H_0)\frac{Z_1}{Z_3}\right] + \frac{Z_1 Z_2}{Z_3 Z_4}} \tag{1.47}$$

Sallen-Key low-pass filter

A low-pass filter is easily obtained from this circuit. Figure 1.15 shows a Sallen-Key low-pass filter.

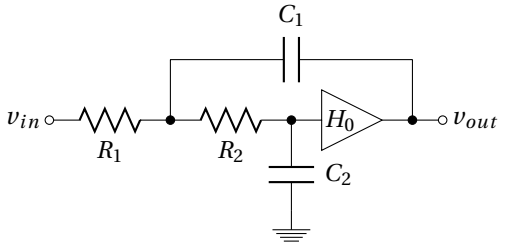


Figure 1.15: Sallen-Key low-pass filter.

The transfer function of this Sallen-Key low-pass filter is given by equation 1.48.

$$\begin{aligned} H_{SK_{LP}} &= \frac{H_0}{1 + \left[(R_1+R_2)C_2 + R_1C_1(1-H_0)\right]s + R_1R_2C_1C_2s^2} \\ &= \frac{H_0}{c_0 + c_1 s + c_2 s^2} \\ &= \frac{H_0}{1 + j\frac{1}{Q}\frac{f}{SFf_c} - \frac{f^2}{SF^2 f_c^2}} \quad \text{with} \quad \begin{cases} SFf_c = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} \\ Q = \frac{\sqrt{R_1R_2C_1C_2}}{(R_1+R_2)C_2 + R_1C_1(1-H_0)} \end{cases} \end{aligned} \tag{1.48}$$

This second order Sallen-Key filter can be used to realize one complex-pole pair in the transfer function of a low-pass cascading filter. Values of the Sallen-Key circuit could be chosen to correspond to a polynomials coefficients (as Butterworth, Chebyshev or Bessel ...).

Sallen-Key high-pass filter

To transform a low-pass filter to a high-pass filter, all resistors are replaced by capacitors and capacitors by resistors :

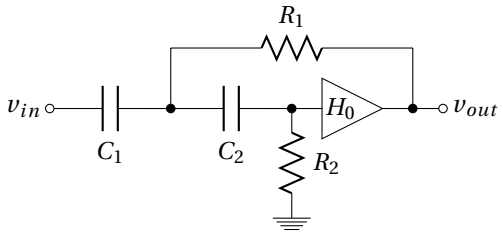


Figure 1.16: Sallen-Key high-pass filter.

The transfer function of this Sallen-Key high-pass filter is given by equation 1.49.

$$\begin{aligned} H_{SK_{HP}} &= H_0 \frac{R_1 R_2 C_1 C_2 s^2}{1 + \left[R_1(C_1 + C_2) + R_2 C_2 (1 - H_0)\right] s + R_1 R_2 C_1 C_2 s^2} \\ &= \frac{H_0}{c_0 + \frac{c_1}{s} + \frac{c_2}{s^2}} = \frac{H_0 \frac{c_2}{c_0} s^2}{c_0 + \frac{c_1 c_2}{c_0} s + c_2 s^2} \\ &= \frac{H_0 \frac{-f^2}{SF^2 f_c^2}}{1 + j\frac{1}{Q}\frac{f}{SFf_c} - \frac{f^2}{SF^2 f_c^2}} \quad \text{with} \quad \begin{cases} SFf_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \\ Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1(C_1+C_2)+R_2 C_2(1-H_0)} \end{cases} \end{aligned} \tag{1.49}$$

Sallen-Key band-pass filter

Band-pass filter could be obtained by placing in series a hight and a low pass filter as illustrated in figure 1.17. Cut-off frequency of the low-pass filter need to be higher than the high-pass one ; unless you want to make a resonant filter.

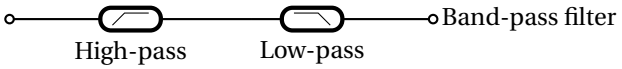


Figure 1.17: Cascading high and low-pass filter for band-pass filtering.

A possible arrangement of generic Sallen-Key topology in band-pass configuration is given in figure 1.18.

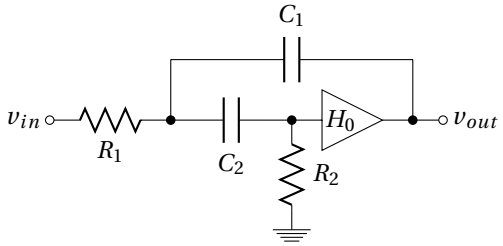


Figure 1.18: Sallen-Key band-pass filter.

But we can also found more complicated band-pass filter as figure 1.19 based on voltage-controlled voltage-source (VCVS) filter topology which gives the transfer function expressed in equation 1.50.

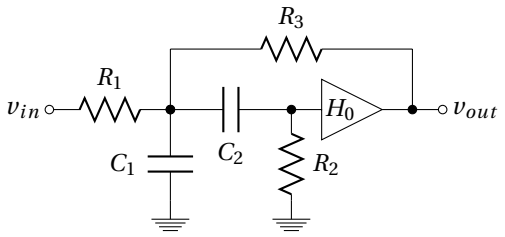


Figure 1.19: Voltage-controlled voltage-source (VCVS) filter topology band-pass filter.

$$\begin{aligned} H_{VCVS_{BP}} &= H_0 \frac{\frac{R_2R_3C_2}{R_1+R_3}s}{1+\frac{R_1R_3(C_1+C_2)+R_2R_3C_2+R_1R_2C_2(1-H_0)}{R_1+R_3}s+\frac{R_1R_2R_3C_1C_2}{R_1+R_3}s^2} \\ &= \frac{H_0' s}{c_0+c_1 s+c_2 s^2} \quad \text{with} \quad H_0' = H_0\frac{R_2R_3C_2}{R_1+R_3} \\ &= \frac{H_0' s}{1+j\frac{1}{Q}\frac{f}{SFf_c}-\frac{f^2}{SF^2f_c^2}} \quad \text{with} \quad \begin{cases} SFf_c = \frac{1}{2\pi}\sqrt{\frac{R_1+R_3}{R_1R_2R_3C_1C_2}} \\ Q = \frac{\sqrt{(R_1+R_3)R_1R_2R_3C_1C_2}}{R_1R_3(C_1+C_2)+R_2R_3C_2-R_1R_2C_2(1-H_0)} \end{cases} \end{aligned} \tag{1.50}$$

Sallen-Key band-reject filter

Unlike the band-pass filter, a notch filter can not be obtained by a series connection of low and high-pass filters. But a summation of the output * of a low and a high-pass filter could be a band-reject filter if cut-off frequency of the low-pass filter is lower than the high-pass one. This correspond to paralleling high and low-pass filter.

Band-reject filter could be obtained by placing in parallel a high and a low-pass filter as illustrated in figure 1.20.

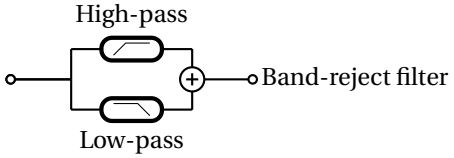


Figure 1.20: Paralleling low and high-pass filter for band-reject filtering.

A band-reject filter is usualy obtained by using circuit of figure 1.21.
Parameters of this simplified Sallen-Key band reject filter is given by expression 1.51.

$$\begin{aligned} SFf_c &= \frac{1}{2\pi\sqrt{RC}} \\ Q &= \frac{1}{4-2H_0} \end{aligned} \tag{1.51}$$

*In practice it is not possible to connect together two outputs without precautions.

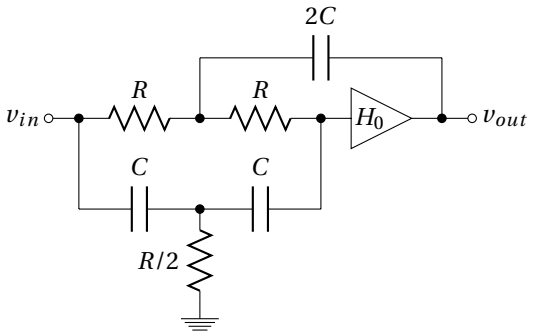


Figure 1.21: Sallen-Key band-reject filter.

1.5 Amplitude responses

1.5.1 Filter specifications

The more common filter specification is the **roll-off rate** which increases with the order [*].
It is 20dB/decade per pole for hight and low-pass filter ; per pair of poles/zeros for band-pass filter.
Ripples in pass-band and stop-band need to be also specified. Around a cutoff frequency, these specifications could be also defined by 5 transfer function requirements :

- maximum amplitude $|H|_{max}$ [†]
- pass-band cut-off frequency f_p [‡]
- maximum allowable attenuation in the band-pass A_{max} [§]
- frequency at which stop-band begins f_s
- minimum allowable attenuation in the stop-band A_{min}

Figure 1.22 lets appear these various parameters in the case of a low pass filter :

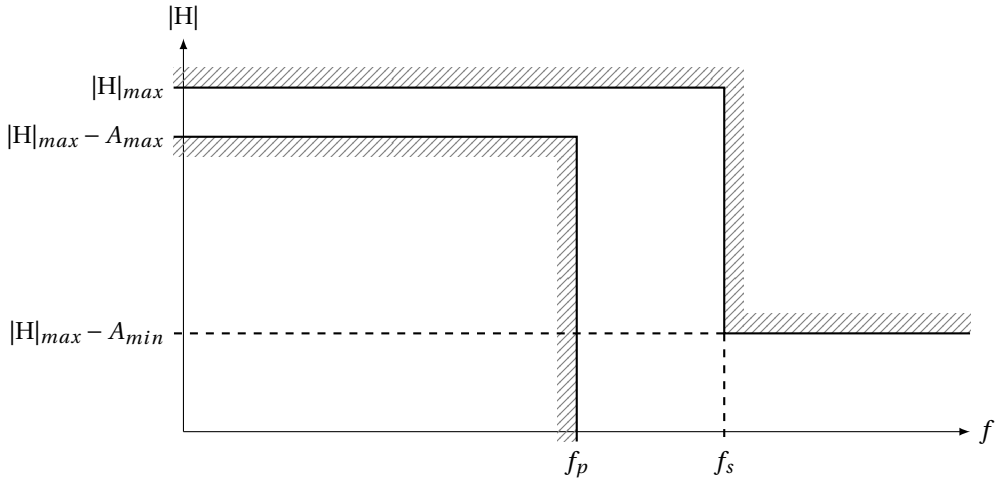


Figure 1.22: Filter amplitude response limits.

[*]The order of the filter is linked to the number of elements (first and second order filter) used in the network (Fig. 1.10).
[†]in the case of low-pass filter, $|H|_{max} = H_0$ the DC gain and H_∞ in the case of high-pass filter $|H|_{max}$, is generally equal to 1.
[‡]for a $-3dB$ attenuation A_{max}, f_p is the cutoff frequency usually noted f_c.
[§]$A_{max} = 3dB$ in the case of Butterworth or Bessel filter and $A_{max} = \frac{1}{\sqrt{1+\epsilon^2}}$ for Chebyshev filter.

1.5.2 Amplitude response curves

Cebyshev filter has a steeper rolloff near the cutoff frequency when compared to Butterworth and Bessel filters. While, Bessel not exhibit a frequency dependance phase shift as Butterworth and Chebyshev filter. Butterworth is a good compromise as regards to the rolloff, while having a maximaly-flat frequency response. Finally, Legendre filter has the steeper rollof without ripple in the band pass. These kind of comparison between Butterworth, Chebyshev, Bessel and Legendre filter is outlined by figure 1.23, tables 1.8 and 1.9.



Figure 1.23: Steepness and phase linearity filter comparison.

Filter \ Properties	Advantages	Disadvantages
Butterworth	Maximally flat magnitude response in the pass-band	Overshoot and ringing in step response
Chebyshev	Better attenuation beyond the pass-band	Ripple in pass-band. Even more ringing in step response
Bessel	Excellent step response	Even poorer attenuation beyond the pass-band
Legendre	Better rolloff without ripple in pass-band	pass-band not so flat

Table 1.8: Butterworth, Chebyshev, Bessel and Legendre filter advantages/disadvantages.

Properties \ Filter	Butterworth	Chebyshev	Bessel	Legendre
roll-off rate for a given order	average	**good**	weak	average
group delay	good	bad	**excellent**	average
flatness of the frequency response	**excellent**	ripple in the pass-band	excellent	good
transient response	good	average	excellent	good

Table 1.9: Butterworth, Chebyshev, Bessel and Legendre filter comparison.

The response of Butterworth, Chebyshev, Bessel and Legendre low-pass filter is compared. To do this, polynomial tables given in Appendix A are directly used as the low-pass filter **denominator** transfer function. Figure 1.24 shows for example the 5^{th} order of Butterworth, Chebyshev, Bessel and Legendre polynomials as a denominator ; only the module (expression 1.52) is plotted.

$$
\begin{aligned}
P_{5_{\text{Butterworth}}} &= (s+1)(s^2+0.618s+1)(s^2+1.618s+1)\\
P_{5_{\text{Chebyshev}_{3dB}}} &= (5.6328s+1)(2.6525s^2+0.7619s+1)(1.0683s^2+0.1172s+1)\\
P_{5_{\text{Bessel}}} &= (0.665s+1)(0.3245s^2+0.6215s+1)(0.4128s^2+1.1401s+1)\\
P_{5_{\text{Legendre}}} &= (2.136s+1)(1.0406s^2+0.3196s+1)(2.0115s^2+1.5614s+1)
\end{aligned}
$$

$$
|P_5| = \begin{cases}
\sqrt{\left(\frac{f^2}{f_c^2}+1\right)\left(\left(\frac{f^2}{f_c^2}+1\right)^2+0.618^2\frac{f^2}{f_c^2}\right)\left(\left(\frac{f^2}{f_c^2}+1\right)^2+1.618^2\frac{f^2}{f_c^2}\right)} \\
\sqrt{\left(5.6328^2\frac{f^2}{f_c^2}+1\right)\left(\left(2.6525\frac{f^2}{f_c^2}+1\right)^2+0.7619^2\frac{f^2}{f_c^2}\right)\left(\left(1.0683\frac{f^2}{f_c^2}+1\right)^2+0.1172^2\frac{f^2}{f_c^2}\right)} \\
\sqrt{\left(0.665^2\frac{f^2}{f_c^2}+1\right)\left(\left(0.3245\frac{f^2}{f_c^2}+1\right)^2+0.6215^2\frac{f^2}{f_c^2}\right)\left(\left(0.4128\frac{f^2}{f_c^2}+1\right)^2+1.1401^2\frac{f^2}{f_c^2}\right)} \\
\sqrt{\left(2.136^2\frac{f^2}{f_c^2}+1\right)\left(\left(1.0406\frac{f^2}{f_c^2}+1\right)^2+0.3196^2\frac{f^2}{f_c^2}\right)\left(\left(2.0115\frac{f^2}{f_c^2}+1\right)^2+1.5614^2\frac{f^2}{f_c^2}\right)}
\end{cases}
\tag{1.52}
$$

It clearly appears on figure 1.24 differences, concerning frequency response, between Butterworth, Chebyshev, Bessel and Legendre filters. All these filters have been plotted with a cutoff frequency referred to a -3dB attenuation. Thereby, despite the same order, Chebyshev filter has the faster rolloff, then come Legendre, Butterworth and the slower is the Bessel filter. **Far after the cutoff frequency, the slope becomes the same for all 5^{th} order filters ($\propto f^{-5}$) but not the attenuation** for a given $\frac{f}{f_c}$.

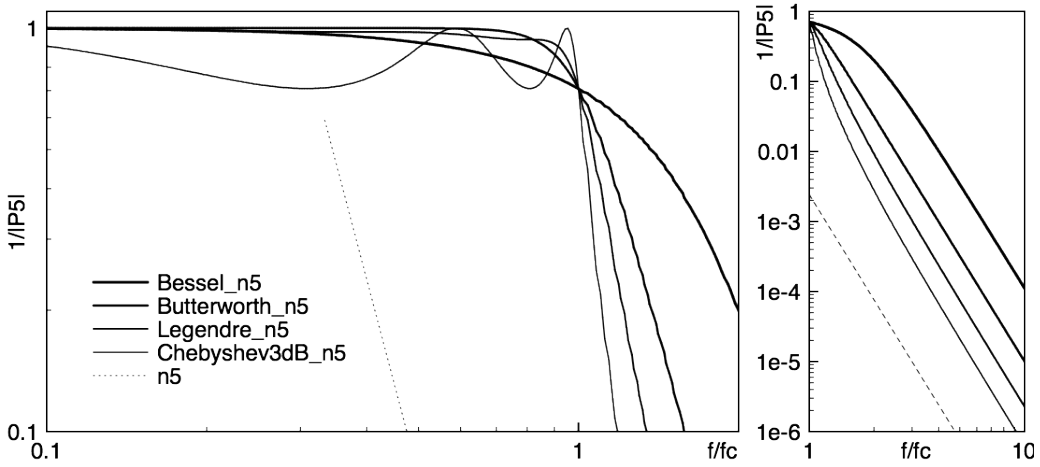


Figure 1.24: Frequency response of a Butterworth, Chebyshev, Bessel and Legendre 5^{th} order low-pass filter around cutoff frequency and far after it. Dashed line represent a f^{-5} slope for comparison to 5^{th} order filter rolloff.

The drawback of a fast rolloff is the increasing of the transit time to step response as shown in figure 1.25. Time response of a Chebyshev filter clearly shows oscillations which increase the settling time*.

Butterworth frequency response

Figure 1.26 illustrates the main properties of Butterworth filters which is the flatness in the pass-band ; particularly for high order.

Butterworth attenuation plot on the right side of figure 1.26 could be used to determined the needed order for a given A_{min} and f_s (Fig. 1.22).

*Settling time is the time requires to reach and stay around the final voltage with a specified errors; usually a range of 1%, 2% or 5%

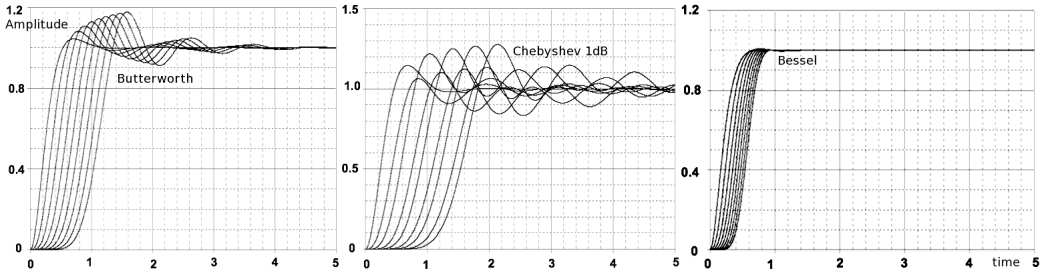


Figure 1.25: Normalized ($f_c = 1$) time response (step) of multipole (2 to 10) Butterworth, Chebyshev 1dB and Bessel low-pass filters.

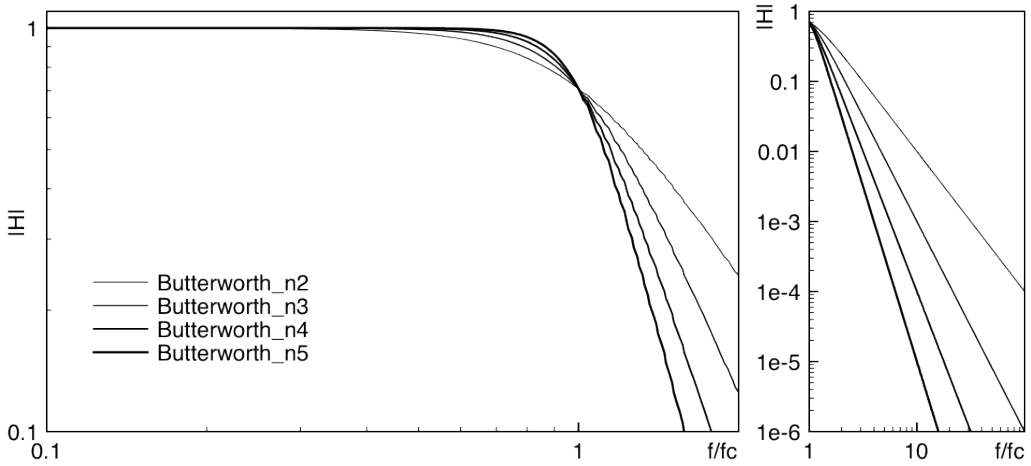


Figure 1.26: Frequency response of a Butterworth low-pass filter for n = 2 to 5.

Chebyshev frequency response

Figure 1.27 shows the ripple in the pass-band of a Chebyshev low-pass filter (3dB) for order from 2 to 5. It also appears that H_0 (numerator) is different from 1 for **even order**. For an even order Chebyshev filter with a ripple factor of 3 dB (which correspond to $\epsilon = 1$), the numerator is equal to $\frac{1}{\sqrt{1+\epsilon^2}} \approx 0.71$.

Figure 1.28 shows more precisely the difference in H_0 between odd (n=5 $\rightarrow$ $H_0 = 1$) and even (n=4 $\rightarrow$ $H_0 \approx 0.707$) order. It also illustrates of how it is possible to determine the order of a Chebyshev filter by simply counting the ripple number on the transfer function.

Amplitudes of the ripples in the pass-band is constrained by the $|H|_{max} - A_{max}$ and f_c (Fig. 1.22). Sometimes, ripple factor needs to be smaller than 3dB. It is easy to find Chebyshev polynomials table with a ripple factor of 1 dB*, 0.5 dB or 0.1 dB. In Figure 1.29, is plotted the transfer function of a Chebyshev low-pass filter with a ripple factor of 1 dB ($\epsilon = 0.5$) and order going from 2 to 5. The H_0 of even order is set at $\frac{1}{\sqrt{1+0.5^2}} \approx 0.894$ as it is shown in figure 1.30.

Finally, a comparison between two Chebishev low-pass filters with different ripple factor is plotted in figure 1.31. Even if the cutoff frequency is referred to a different level (-1 dB and -3 dB), it appears that the larger the ripple factor, the faster the rolloff.

Bessel frequency response

Figure 1.32 show Bessel low-pass filter transfer function from the 2^{nd} to the 5^{th} order. The rolloff is much slower than for other filters. Indeed, Bessel filter maximizes the flatness of the group delay curve in the pass-band (Fig. 1.33) but not the rolloff. So, for a same attenuation in the stop-band (A_{min}), a higher order is required compared to Butterworth, Chebyshev or Legendre filter.

*Chebyshev polynomials table is given in Appendix A for a ripple factor of 3 and 1 dB

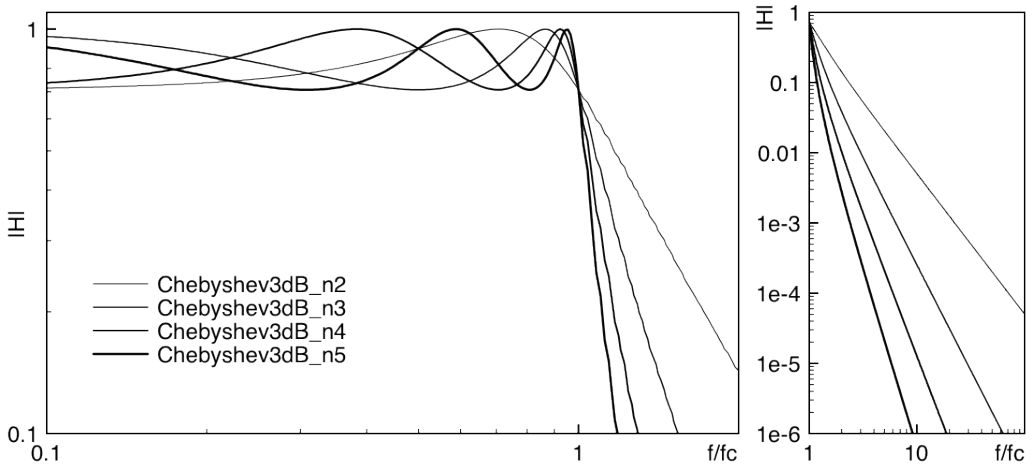


Figure 1.27: Frequency response of a Chebishev ($\epsilon = 1$) low pass filter for n = 2 to 5.

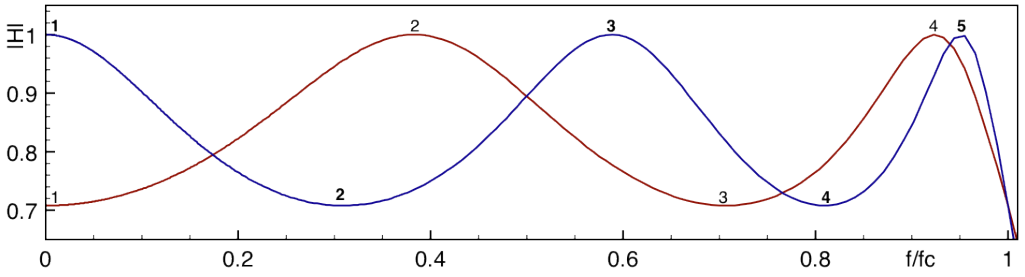


Figure 1.28: Zoom in the passband of the frequency response of a Chebishev ($\epsilon = 1$) low-pass filter for n = 4 and 5.

Legendre frequency response

To complete this inventory, Legendre low-pass filter frequency response is plotted in figure 1.34 for n = 2 to 5.

Legendre filter is characterized by the maximum possible rolloff consistent with monotonic magnitude response in the pass-band. But monotonic does not flat, as we can see in figure 1.35.

As for Chebyshev filter, it is possible to count the number of "ripples" to find the order from a plotted transfer function.

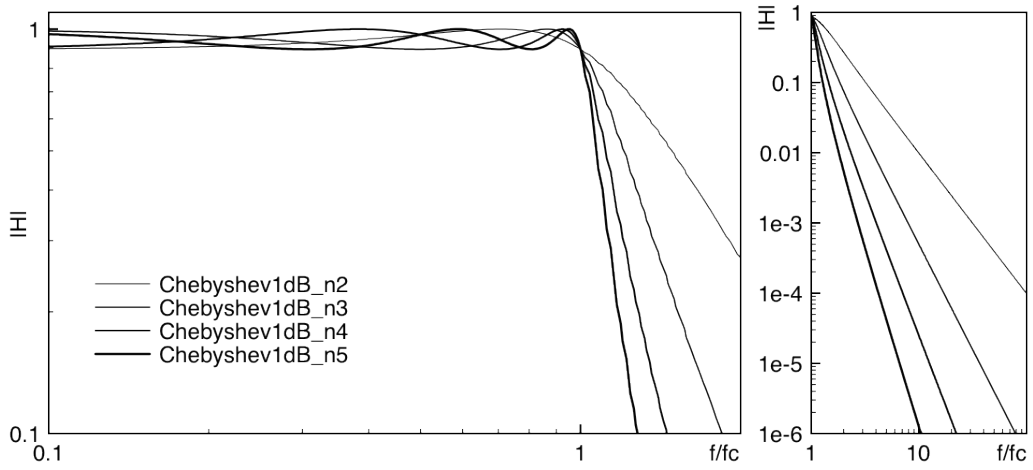


Figure 1.29: Frequency response of a Chebishev ($\epsilon = 0.5$) low-pass filter for n = 2 to 5 order filter rolloff.

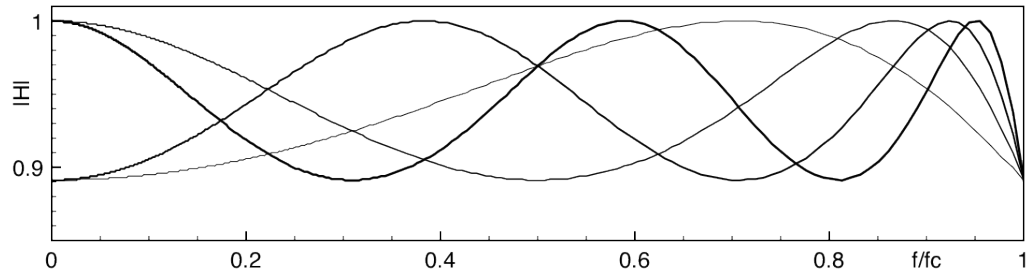


Figure 1.30: Zoom in the pass-band of the frequency response of a Chebishev ($\epsilon = 0.5$) low-pass filter for n = 2 to 5.

1.6 Switched capacitor filters

A switched capacitor electronic circuit works by moving charges into and out of capacitors when switches are opened and closed. Filters implemented with these elements are termed "switched-capacitor filters".

1.6.1 Switched capacitor

Figure 1.36 give the circuit of a switched capacitor resistor, made of one capacitor C and two switches S_1 and S_2 which connect the capacitor with a given frequency alternately to V_{in} and V_{out}. Each switching cycle transfers a charge from the input to the output at the switching frequency. When S_1 is closed while S_2 is open, the charge stored in the capacitor C is $q_{in} = CV_{in}$ [*], when S_2 is closed, some of that charge is transferred out of the capacitor, after which the charge that remains in capacitor C is $q_{out} = CV_{out}$.

Thus, the charge moved out of the capacitor to the output is $q_T = q_{in} - q_{out} = C(V_{in} - V_{out})$. Because this charge q_T is transferred each T_S[†], the rate of transfer of charge per unit time [‡] is given by expression 1.53.

$$I = \frac{q_T}{T_S} = \frac{C(V_{in} - V_{out})}{T_S} \tag{1.53}$$

Expression 1.53 gives a link between V and I, and then the impedance [§] of the switched capacitor

[*] q=CV, q the charge on a capacitor C with a voltage V between the plates.
[†] T_S Periodicity of switch opening and closing.
[‡] The rate of flow of electric charge is a current I[A].
[§] The impedance of the capacitor could be considered static for a frequency smaller than $\frac{1}{T_S}$.

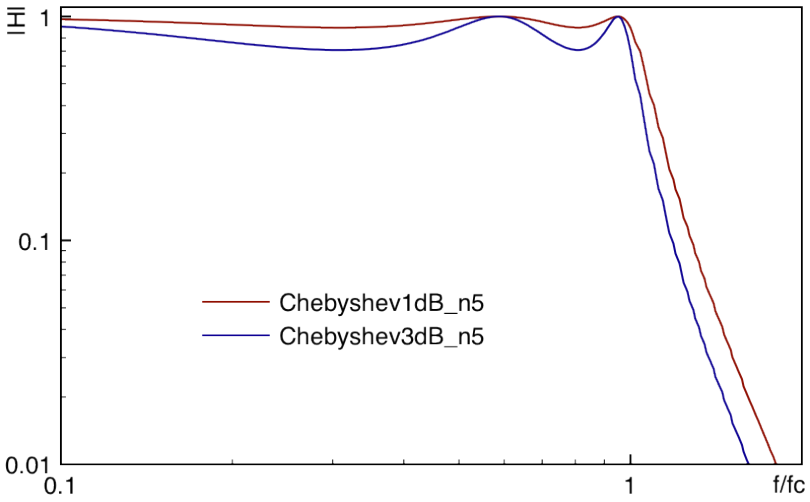


Figure 1.31: Comparison between frequency response of two Chebishev low-pass filters of 5^{th} order, one with a ripple factor of 1 dB, and the other with 3 dB.

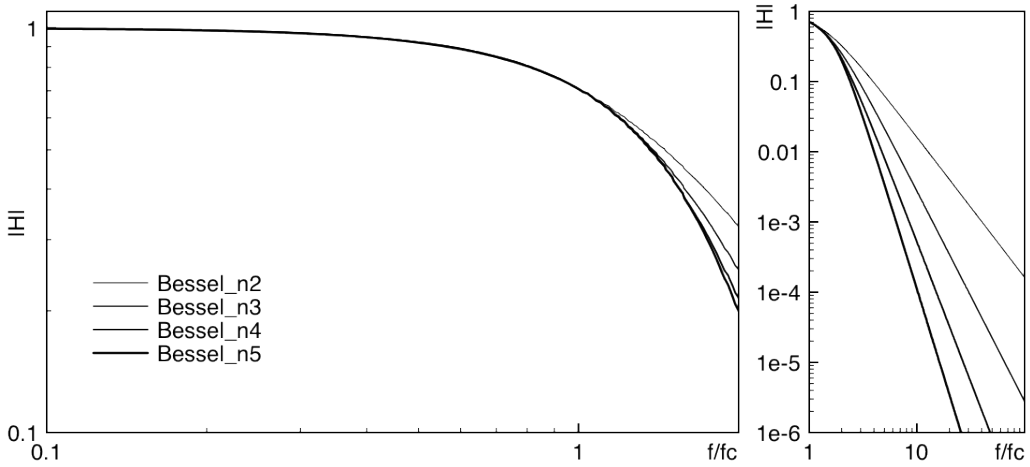


Figure 1.32: Frequency response of a Bessel low-pass filter for n = 2 to 5.

which could be expressed as a resistor (expression 1.54).

$$R = \frac{T_s}{C} \tag{1.54}$$

Switching capacitor behaves like a lossless resistor whose value depends on capacitance C and switching frequency $\frac{1}{T_S}$. This reduces energy consumption for embedded applications (such as space mission) and allows an adjustment of the resistance value.

1.6.2 Switched capacitor filters

Because switching capacitor act as a resistor, **switched capacitors can be used instead of resistors** in the previous filter circuits (RC, RLC, Sallen-Key ...). A $R = 10k\Omega$ can be replaced by a switched capacitor following the expression 1.54. Using a switching clock $f_s = \frac{1}{T_S} = 50kHz$, the capacitor is given by equation 1.55.

$$R = 10k\Omega \quad \equiv \quad C = \frac{1}{10k\Omega \times 50kHz} = 2nF \tag{1.55}$$

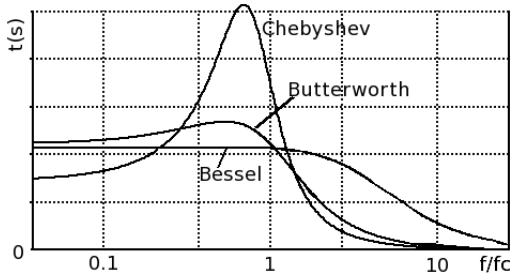


Figure 1.33: Comparison of the delay time as a function of frequency $\left(\frac{f}{f_c}\right)$ between a Bessel, a Butterworth and a Chebyshev low-pass filter (n=4).

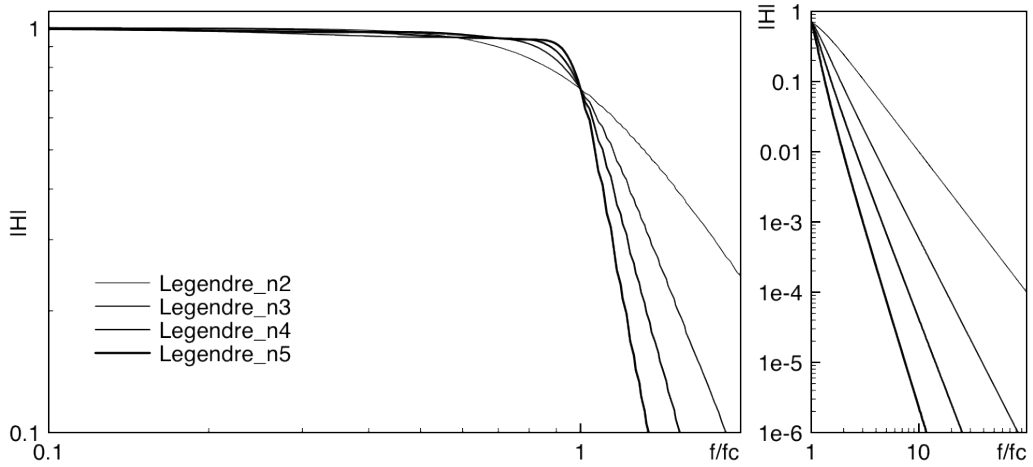


Figure 1.34: Frequency response of a Legendre low-pass filter for n = 2 to 5

A variation of the switching frequency leads to a variation of the equivalent resistance R. If f_s increases, $R = \frac{1}{C \times f_s}$ decreases. This link between frequency and equivalent resistance value could be used to modify a filter cutoff frequency by adjusting the switching frequency.

The cutoff frequency of a RC switched capacitor filter (Fig. 1.37) is expressed by equation 1.56.

$$f_c = \frac{1}{2\pi R_{equiv.} C_2} = \frac{C_1 \times f_s}{2\pi C_2} \tag{1.56}$$

If the switching frequency f_s increases, the cutoff frequency f_c increases too.

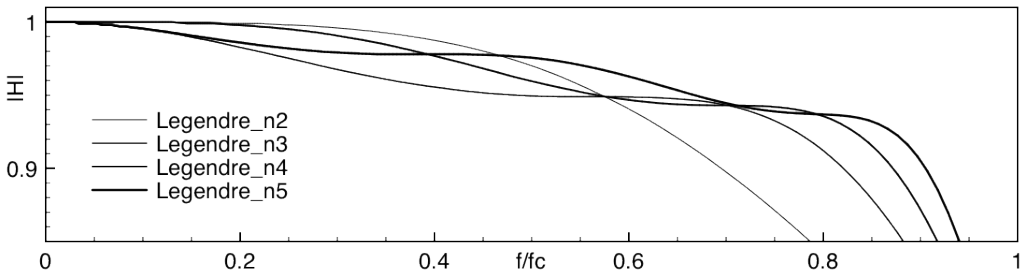


Figure 1.35: Zoom on the pass-band of the frequency response of a Legendre low-pass filter for n = 2 to 5.



Figure 1.36: Equivalence between Resistor and Switched Capacitor.

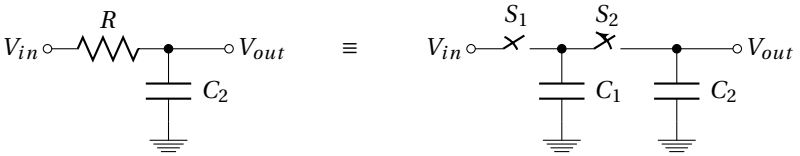


Figure 1.37: Equivalence between RC filter and switched capacitor filter.

Tutorial

1.7 First order passive filter

Transfer function of the first order filter (Fig. 1.38).

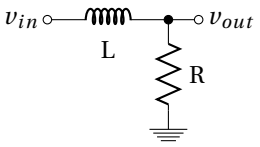


Figure 1.38: First order LR filter.

1. Give the expression of the $\frac{v_{out}(\omega)}{v_{in}(\omega)}$ transfer function.
2. Is it a low or a high-pass filter?

   $R = 1k\Omega$ and $L = 1mH$:
3. What is the cutoff frequency?
4. Give the module and the phase of this transfer function as a function of f.
5. Draw the Bode plots of the filter.
6. Same questions for the two following filters :
   $R = 22k\Omega$ and $C = 33nF$



Figure 1.39: 2 other First order filters.

1.8 Second order passive filter

Transfer function of the second order filter (Fig. 1.40).
$L = 1mH$, $R = 1\Omega$ and $C = 100nF$:

1. Give the expression of the $\frac{v_{out}(\omega)}{v_{in}(\omega)}$ transfer function highlighting the damping factor ζ.
2. Compute the cutoff frequency and the damping factor
3. Express the module and the phase of this transfer function.
4. Draw the Bode plots of the filter.
5. Is it a low or a high-pass filter?
6. What is the values of R which satisfy $\zeta = 0.71$, $\ll 1$ and $\gg 1$?
7. Is the cutoff frequency changes with R values?
8. Draw the Bode plots of the filter with $\zeta = 0.71$, $\ll 1$ and $\gg 1$.
9. What is the correspondence between ζ and Q ?

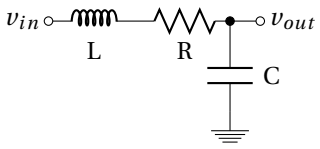


Figure 1.40: Second order LRC filter.

1.9 Active filter - Sallen-Key topology

Sallen-Key topology is given in Fig. 1.41.

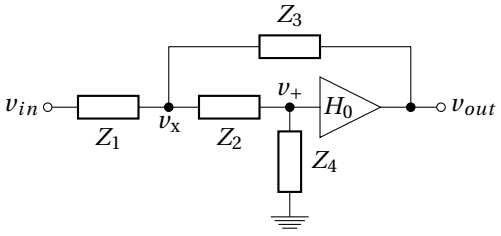


Figure 1.41: Sallen-Key generic topology.

Find the transfer function of the Sallen-Key topology using Kirchhoff's current law :

1. Give the link between v_+ and v_{out}.
2. Apply the Kirchhoff's current law to the v_x node.
3. Apply the Kirchhoff's current law to the v_+ node.
4. Use 1) and 3) to give an expression of v_x as a function of v_{out}.
5. Use 2) and 4) to give an expression of v_{out} as a function of v_{in}.
6. Rearrange equation from 5) to obtain $\frac{v_{out}}{v_{in}}$ transfer function as in the Lecture.

1.10 5^{th} order Butterworth low-pass filter

1. Give the transfer function of a 5^{th} order Butterworth low-pass filter by using polynomials table from Appendix A.
2. What is the number of filter stages required, and the order of each. Give Q and SFf_c for each second order.
3. Suggest a circuit, using cascading and Sallen-Key topology. Give the expression of each cutoff frequency and quality factor as a function of R and C values.

1.11 4^{th} order Chebyshev (3dB) low-pass filter

- Same question as before, to build a 4^{th} order Chebyshev low-pass filter.

1.12 6^{th} order Bessel high-pass filter

- Same question as before, to build a 6^{th} order Bessel high-pass filter.

1.13 Filter synthesis from template

1.13.1 Low pass-filter synthesis

We search to build a low pass filter to satisfy the following specifications :

- maximum amplitude $|H|_{max} = 0\ dB$
- pass-band cut-off frequency $f_c = 5\ kHz$
- maximum allowable attenuation in the band-pass $A_{max} = 3\ dB$
- frequency at which stop-band begins $f_s = 20\ kHz$
- minimum allowable attenuation in the stop-band $A_{min} = 40\ dB$

The template of this filter is given in figure 1.42.

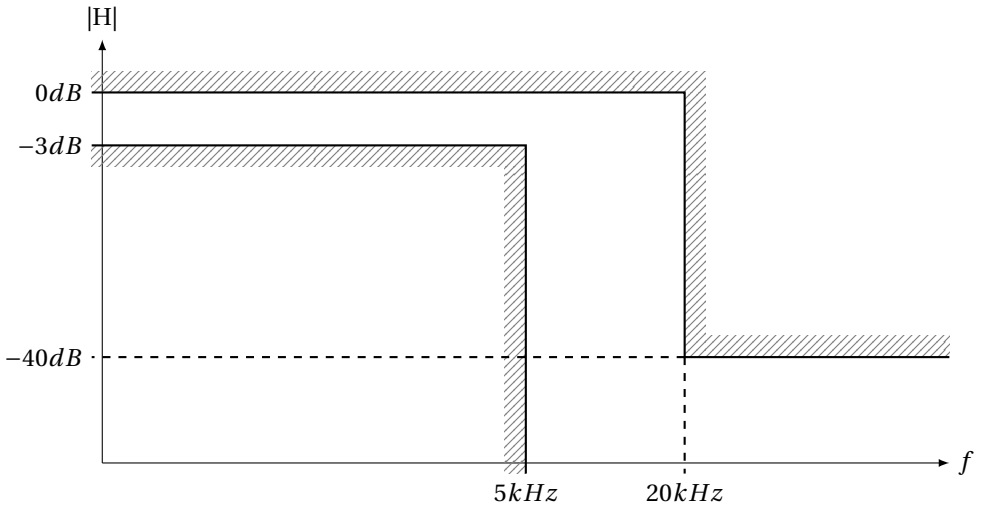


Figure 1.42: Low pass filter specifications.

1. What is the minimum filter order needed to satisfy previous constraints. Consider, Butterworth and Chebyshev 1 dB filters. Use plots given in Appendix B to graphically estimate attenuation of different filters.

2. From these 2 filters, what is the one which exhibit a 10% settling time* smaller than $330\mu s$. Use step responses given in Lecture to estimate settling time. For Chebyshev, consider the 1dB response time.

   $R_0 = 10k\Omega$, $\omega_c = \frac{1}{R_0\sqrt{C_1C_2}}$, $H_0 = 1$ and $Q = \frac{\sqrt{C_1C_2}}{2C_2}$

3. Give the circuit (and the capacitor values, SF and Q) of the filters Butterworth n=4 using Sallen-Key topology (for 2^{nd} order filters) given in figure 1.43.

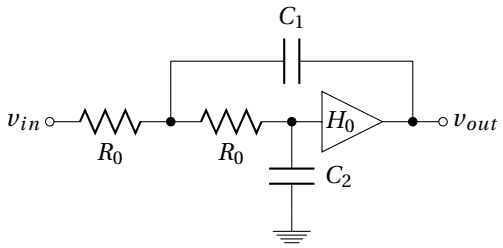


Figure 1.43: Sallen-Key 2^{nd} order low-pass filter. R1 = R2 = R0

This circuit is now used to filter a 500 Hz square signal before a 10 kHz digitizer. The filter is needed to avoid aliasing but shall not add distortions.

1.13.2 Removing harmonics frequencies

Saturations and distortions generate unwanted harmonics that we search to suppress by filtering.

1. Consider the distorted signal as a square one (at frequency f_{in}) and the number 3 harmonic† as the main distortion. Suggest filter specifications (in the same manner as figure 1.42) to have the harmonic$_3$ 60 dB smaller than fundamental signal.

2. What is the minimum order required for each type of filter (Butterworth, Chebyshev, Bessel, Legendre)?

3. Choose filter which require the smaller order and give circuit from Sallen-Key topology ($f_0 = f_{in} = 1kHz$ and $R_0 = 10k\Omega$)

*Settling time is the time required to get within some specified amount of the final value (10% here) and stay there. This is different from rise time which is the time required to reach 90% of the final value.

†Harmonic$_3$ is the harmonic at 3 times the fundamental frequency f_{in}

Lab work

1.14 Passive filter



Figure 1.44: First order filters.

1. Implement the 2 RC circuits (Fig. 1.44) and measure Bode diagram (amplitude and phase) by using a sine wave (from a function generator) and an oscilloscope. $R = 22k\Omega$ and $C = 33nF$.
2. What type of filters is it ? Low or high pass filters?
3. Now, connect in series this two circuit as in figure 1.45. What kind of filter do you obtain?
4. Mesure its characteristics in the two cases. Draw the Bode diagram. Comment the difference between the two circuits.
5. Same questions with circuit connected as figure 1.46.
6. Place a voltage follower between the two stages for figure 1.45 and 1.46 circuits (Aop are TL081 biased under $\pm 12\ V$). Comment.

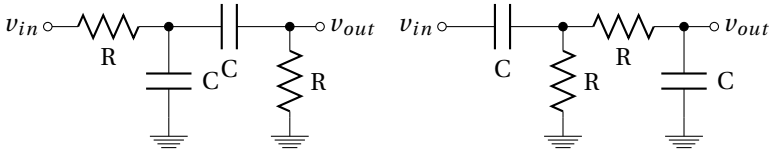


Figure 1.45: First order filters in series.

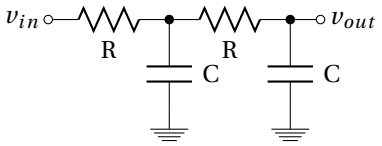


Figure 1.46: 2 First order filters in series.

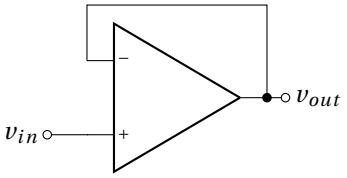


Figure 1.47: Voltage follower. $v_{out} = v_{in}$ with impedance matching ($Z_{in} \approx \infty$ and $Z_{out} \approx 0$).

1.15 Low pass-filter synthesis

We search to build a low pass filter to satisfy the following specifications :

- maximum amplitude $|H|_{max} = 0\ dB$
- pass-band cut-off frequency $f_c = 5\ kHz$
- maximum allowable attenuation in the band-pass $A_{max} = 3\ dB$
- frequency at which stop-band begins $f_s = 20\ kHz$
- minimum allowable attenuation in the stop-band $A_{min} = 40\ dB$
- 1% settling time $< 330\ \mu s$

Such specifications are satisfy by using a 4^{th} order Butterworth filter (Fig 1.48).

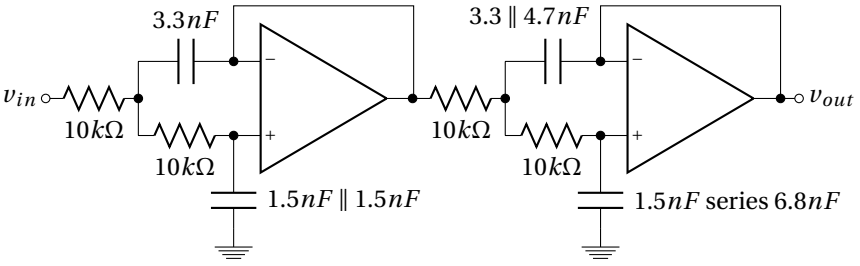


Figure 1.48: Sallen-Key 4^{th} order Butterworth low-pass filter.

1. Implement this circuit (Aop are TL081 biased under $\pm 12\ V$) and measure Bode diagram (amplitude and phase) by using a sine wave (from a function generator) and an oscilloscope. ✐ Add error bars to the graph.
2. We are now considering the phase response. To do this, measure the delay and the phase of the fundamental and the 4^{th} first hamonics* of a 500 Hz square signal. Use a sine wave of 1 V amplitude for each frequencies. ✐ Use 2 probes to measure the delay.
3. Determine the 10% settling time.
4. Change the value of the square signal frequency around the cutoff frequency. comment.

☞ **keep the Butterworth filter**.

*4^{th} first harmonic of a square wave are h_3, h_5, h_7 and h_9

1.16 Removing harmonics frequencies

4^{th} order Chebyshev low pass filter (Fig. 1.49) is used to suppress harmonics of a 1 kHz square signal.

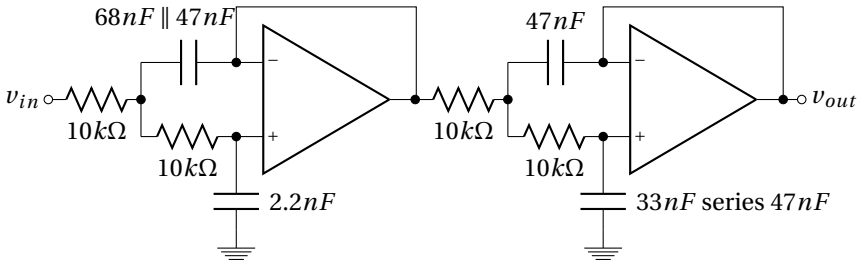


Figure 1.49: Sallen-Key 4^{th} order Chebyshev low-pass filter.

1. Replace capacitors of the Butterworth filter to obtain the Chebyshev filter of figure 1.49. Check quickly performances of the filter : f_c and n.
2. Measure the attenuation of a sine wave at 1 kHz and at 3 kHz. Give the attenuation (at the output of the filter) of the harmonique$_3$ as compared to fundamental of a 1 kHz square signal.
3. Trace the Bode plot of the filter.

☞ Disassemble and clean

Part II

DCDC Converters

2 DC/DC converters

2.1 Introduction

A DC/DC converter is an electronic circuit which converts a Direct Current (DC) source from one voltage level to another. For example, 12 V to 5 V or 12 V to -48 V. Power for a DC/DC converter can come from any suitable DC sources, such as batteries, solar panels, rectifiers and DC generators.

DC/DC converter is a class of switched-mode power supply containing at least two semiconductor switches (a diode and a transistor) and at least one energy storage element, a capacitor, inductor, or both (see for instance the figure 2.3). Filters made of capacitor in combination with inductor reduce output voltage ripple. It is an efficient technique to provide DC voltage as compare to "linear power supplies" presented in figure 2.1.

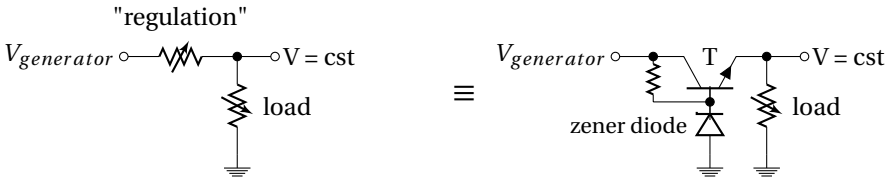


Figure 2.1: *Linear power supplies* topology. A linear power supply regulates the output voltage by continually dissipating power (Joule dissipation) in a pass transistor (made to act like a "variable resistor"). The lost power is $P_{lost} = (V_{out} - V_{in})I_{load}$. The resistance of the regulator varies in accordance with the load, resulting in a constant output voltage (cst). A voltage reference as provide here by the zener diode is also needed. *Regulator* circuits as the well known *TL7805* provide all need devices to do linear regulation in the same package (See Appendix).

2.1.1 Advantages/Disadvantages

Pros :

DC/DC converters offer three main advantages compared to linear regulators :

1. **Efficiency :** Switching power supplies offer higher efficiency than traditional linear power supplies. Unlike a linear power supply, the pass transistor of a switching-mode supply, continually switches between low-dissipation, full-on and full-off [*], states [†], and spends very little time in transitions to minimize wasted energy. Ideally, a switched mode power supply dissipates no power. This higher efficiency is an important advantage of a switched mode power supply.

[*] no resistances, *ie* no voltage drop or no dissipative current

[†] A switching regulator uses an active device that switches "on" and "off" to maintain an average value of output.

2. **Size :** Switched mode power supplies may also be substantially smaller and lighter than a linear supply due to the smaller transformer* size and weight; and due to the less thermal management required because less energy is lost in the transfer.

3. **Output voltages can be greater than the input or negative :** DC/DC converter can transform input voltage to output voltages that can be greater than the input (boost), negative (inverter), or can even be transferred through a transformer to provide electrical isolation with respect to the input. By contrast linear regulator can only generate a lower voltage value than input DC one.

Cons :

However, DC/DC converter are more complicated ; their switching currents can cause electrical noise and interference problems if not carefully suppressed†. Linear regulators provide lower noise ; their simplicity can sometimes offer a less expensive solution. Even if the most of low noise electronic circuits can tolerate some of the less-noisy DC/DC converters ; some sensitive analog circuits require a power supply with so little noise that it can only be provided by a linear regulator.

2.1.2 Applications

DC/DC converter is used in many domestic products to supply whatever voltages are needed in personal computers, mobile phone chargers, as well as in embedded instrument powered by battery and/or solar generator. This is typically used for DC distribution in satellite (see Fig. 2.2). Indeed, **aerospace industry requires small, lightweight, and efficient power converters**.

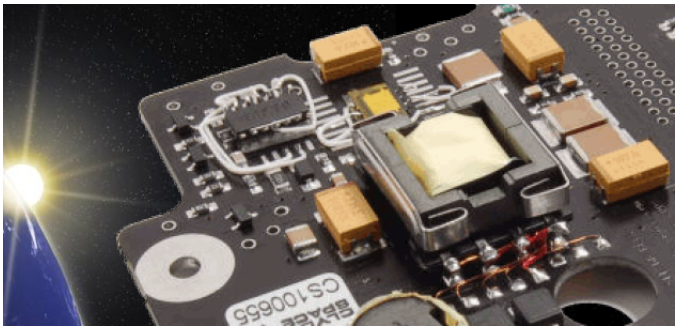


Figure 2.2: DC/DC converter for space applications - CLYDE SPACE

2.2 DC/DC converters

We will discuss 4 different common topologies of DC/DC converter:

1. step-down voltage converter ⇒ *buck* converter.
2. step-up voltage converter ⇒ *boost* converter.
3. inverter voltage converter ⇒ inverting *buck-boost* converter.
4. isolated‡ voltage converter ⇒ *flyback* converter.

*many linear power supplies use large transformer to changes AC amplitude before rectifier diode.

†DC/DC converters have switching noise at the switching frequency and its harmonics. Electrical noise can be emitted from the supplying power lines as RF noise which should be prevented with proper filtering.

2.2.1 *Buck* converters

Buck converter is a **step-down DC/DC converter**. It is composed of an inductor L and two switches (usually a transistor and a diode) that control the inductor charge and discharge (see figure 2.3). Indeed, switches alternate between connecting the inductor to source voltage (store energy in the inductor*) and discharging the inductor into the load.

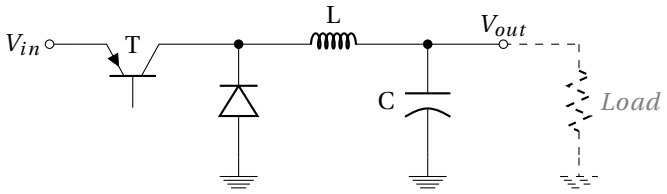


Figure 2.3: *Buck* topology of a step-down DC/DC converter.

It is useful to consider that components are perfect (Fig. 2.4) to simplify the analysis. So the switch and the diode have zero voltage drop when they conduct (*i.e.* ON) and zero current flow when they block (*i.e.* OFF). Moreover, the inductor L has zero series resistance. Further, it is assumed that the input and output voltages do not change over a switching cycle†.

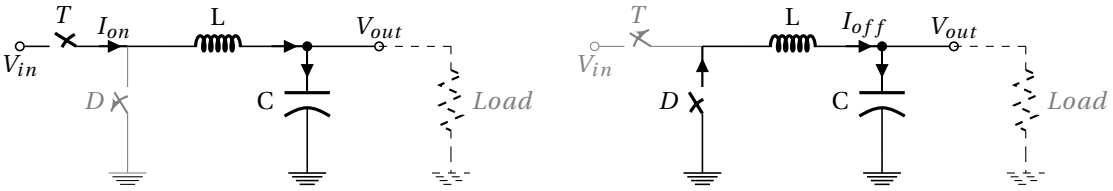


Figure 2.4: Simplified *Buck* converter circuit for the two configurations : left when the transistor T conducts (ON); right when it is OFF.

Continuous operation $\equiv I_L \neq 0 \; \forall \, t$

We consider that the current through the inductor L never falls to zero (continuous mode) during the commutation cycle; this imply minimum switching frequency and capacitor value.

Charge phase T_{ON} : When the transistor conducts (diode is reverse biased), because the inductor current not evolves quickly, the voltage across the inductor ($V_L = V_{in} - V_{out}$) is considered as a constant voltage to a first approximation. So the current through the inductor I_L rises linearly with time following expression 2.1 with a $\frac{V_L}{L}$ slope‡.

$$\mathrm{d}I_L = \frac{1}{L}\int_{t=T_{ON}} V_L \mathrm{d}t \tag{2.1}$$

During the charge phase T_{ON}, I_L increases by the value $\Delta I_{L_{ON}}$ following expression 2.2.

$$\Delta I_{L_{ON}} = \frac{V_{in} - V_{out}}{L} T_{ON} \tag{2.2}$$

*An inductor is a reactor, it reacts to current changes. A current flowing through it leads to a magnetic field in the coil which is equivalent to energy store. If the current changes, the stored magnetic flux opposed a voltage accross the inductor : $v = Ldi/dt$.

†this would imply the output capacitance C being large enough.

‡We consider here the current charge of the inductor. The capacitor is assumed charge at a constant voltage.

Discharge phase T_{OFF} : When the transistor is no longer biased (*i.e.* OFF), diode is forward biased and conducts. The voltage across the inductor becomes equal to $-V_{out}$* and I_L flows to the load through the diode. I_L decreases by the value $\Delta I_{L_{OFF}}$ given by expression 2.3 due to the linear discharge of the inductor.

$$\Delta I_{L_{OFF}} = \frac{-V_{out}}{L} T_{OFF} \tag{2.3}$$

Entire switching cycle : In a steady-state operation condition, I_L at $t = 0$ is equal to I_L at $t = T = T_{ON} + T_{OFF}$. So the increase of I_L during T_{ON} is equal† to the decreasing during T_{OFF}.

$$\Delta I_{L_{ON}} + \Delta I_{L_{OFF}} = 0 \tag{2.4}$$

We can then establish the relationship 2.5 which allows to obtain the conversion factor between V_{in} and V_{out} as a function of the duty cycle $D = \frac{T_{ON}}{T}$. It appears that V_{out} varies linearly with the duty cycle for a given V_{in}.

$$\frac{(V_{in} - V_{out})}{L} T_{ON} - \frac{V_{out}}{L} T_{OFF} = 0 \xrightarrow[D=\frac{T_{ON}}{T_{ON}+T_{OFF}}]{} \boxed{V_{out} = DV_{in}} \tag{2.5}$$

Because the duty cycle D is equal to the ratio between T_{ON} and the period T, it cannot be more than 1. Therefore, $V_{out} \leq V_{in}$. This is why this converter is named a step-down converter.

Figure 2.5 shows the evolution of voltage and current of an ideal *buck* converter during charge and discharge phases.

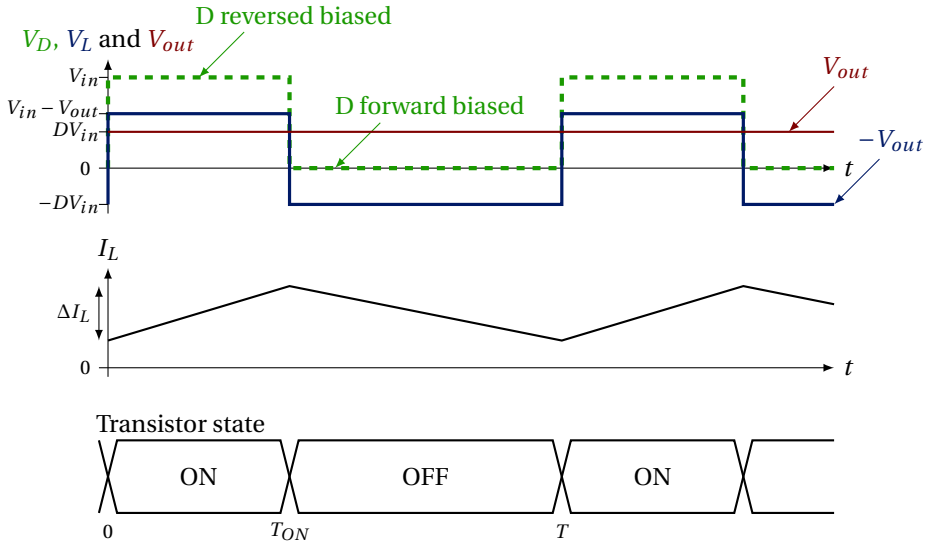


Figure 2.5: Voltages and current as a function of time for an ideal *buck* converter operating in continuous mode *i.e.* I_L never falls to zero..

2.2.2 *Boost* converters

A boost converter (step-up converter) is a DC/DC converter with an **output voltage value greater than its input voltage value**. The key principle that drives the *boost* converter is the tendency of an inductor to oppose to current changes a voltage $v = Ldi/dt$. A schematic of a *boost* converter is shown in figure 2.6.

*Voltage drop across diode is neglected.
†in absolute value, but not in sign.

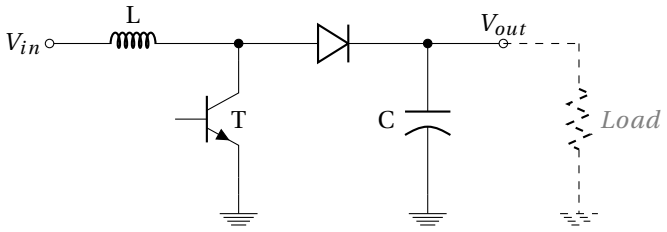


Figure 2.6: *Boost* topology of a step-up DC/DC converter.

When the transistor conduct (*i.e.* ON), the current flows through the inductor and energy is stored in it.

When the transistor block the current (*i.e.* OFF), the energy stored in the inductor L is returned holding the current through it. To do this, the inductor L voltage polarity changes such that it is added to the input voltage. Thus, the voltage across the inductor and the input voltage are in series and they charge together the output capacitor to a voltage higher than the input voltage.

Figure 2.7 shows the evolution of voltage and current of an ideal *boost* converter during charge and discharge phases.

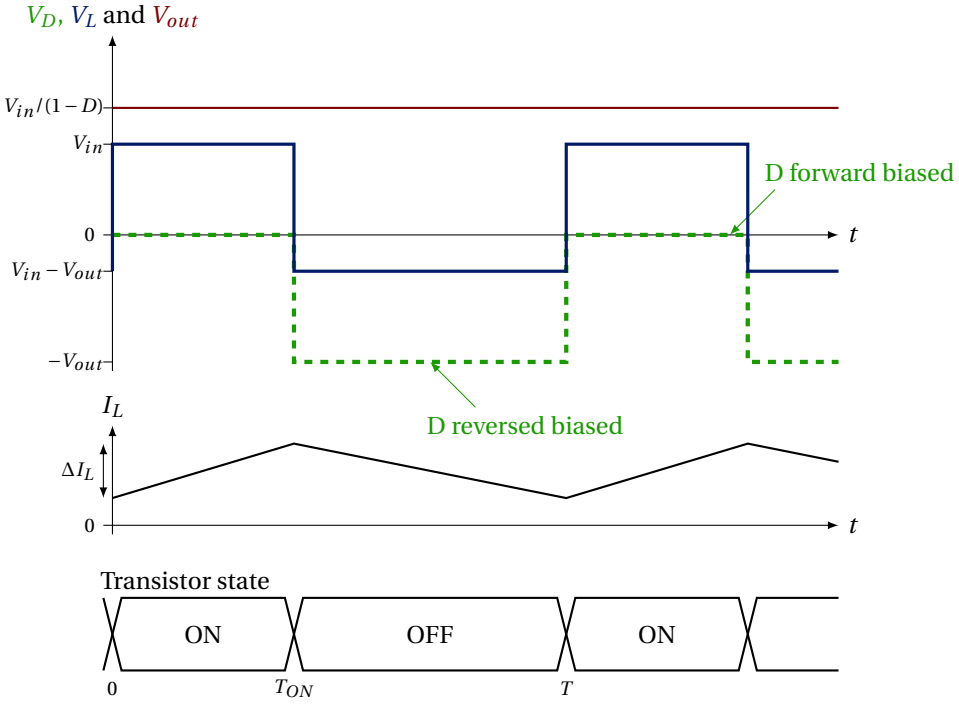


Figure 2.7: Voltages and current as a function of time for an ideal *boost* converter operating in continuous mode *i.e.* I_L never falls to zero.

As for *buck* converter we consider the current through the inductor I_L during the "ON" and "OFF" states :

$$\begin{cases} \Delta I_{L_{ON}} = \frac{1}{L}\int_{t=T_{ON}} V_{in}\mathrm{d}t & = \frac{V_{in}}{L} T_{ON} \\ \Delta I_{L_{OFF}} = \frac{1}{L}\int_{t=T_{OFF}} (V_{in} - V_{out})\mathrm{d}t & = \frac{V_{in}-V_{out}}{L} T_{OFF} \end{cases} \tag{2.6}$$

Over the all switching cycle, the equation 2.4 is again true. so :

$$\Delta I_{L_{ON}} = -\Delta I_{L_{OFF}} \quad \Rightarrow \quad \frac{V_{in}}{L} T_{ON} = \frac{V_{out} - V_{in}}{L} T_{OFF} \quad \Rightarrow \quad V_{out} = V_{in} \frac{T_{ON} + T_{OFF}}{T_{OFF}} \tag{2.7}$$

As for *buck converter*, conversion factor of a *boost* converter could be expressed as a function of the duty cycle $D = T_{ON}/(T_{ON} + T_{OFF})$ and is given in equation 2.8.

$$\boxed{V_{out} = \frac{1}{1-D} V_{in}} \tag{2.8}$$

2.2.3 *Buck-boost* inverting converters

A *Buck-boost* converter is a DC/DC converter that has an output voltage magnitude that is either greater than* or smaller than the input voltage magnitude. The *Buck-boost* converter presented in figure 2.8 is also called inverting converter because its **output voltage is of the opposite polarity as the input**.

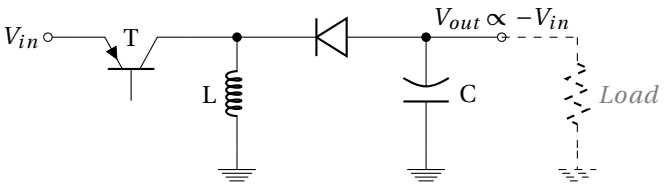


Figure 2.8: *Buck-boost* inverting topology of DC/DC converter. V_{out} is of the opposite polarity as V_{in}.

When the transistor conduct (*i.e.* ON), the input voltage source is directly connected to the inductor. This results in accumulating energy in L. In this step, this is the capacitor C which supplies energy to the output load.

When the transistor blocks (*i.e.* OFF), the inductor is connected to the capacitor, so energy is transferred from L to C and therefore also to the output load.

Figure 2.9 shows the evolution of voltage and current of an ideal *buck-boost* converter during charge and discharge phases.

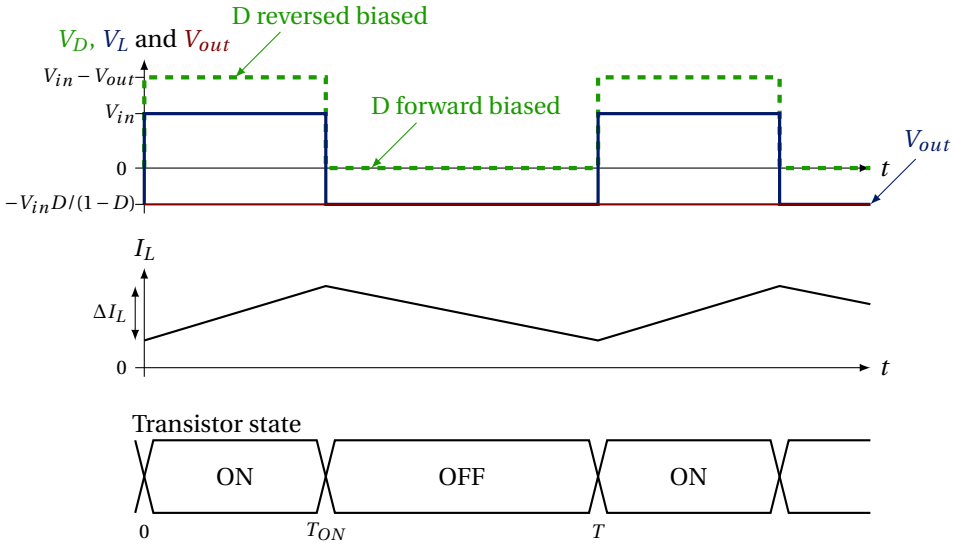


Figure 2.9: Voltages and current as a function of time for an ideal *buck* converter operating in continuous mode *i.e.* I_L never falls to zero..

*in absolute magnitude.

Again, we consider the current I_L during the "ON" and "OFF" states as expressed in equation 2.9.

$$\begin{cases} \Delta I_{L_{ON}} = \frac{1}{L}\int_{t=T_{ON}} V_{in}\mathrm{d}t & = \frac{V_{in}}{L}T_{ON} \\ \Delta I_{L_{OFF}} = \frac{1}{L}\int_{t=T_{OFF}} V_{out}\mathrm{d}t & = \frac{V_{out}}{L}T_{OFF} \end{cases} \tag{2.9}$$

Assuming a continuous mode over the all switching cycle, we consider the increase of I_L during T_{ON} equal to the decreasing during T_{OFF} leading to equalities 2.10 for the *buck-boost* converter.

$$\Delta I_{L_{ON}} = -\Delta I_{L_{OFF}} \quad \Rightarrow \quad -\frac{V_{in}}{L}T_{ON} = \frac{V_{out}}{L}T_{OFF} \quad \Rightarrow \quad V_{out} = -V_{in}\frac{T_{ON}}{T_{OFF}} \tag{2.10}$$

Conversion factor of the *buck-boost* converter is finally given by the equation 2.11 as a function of the duty cycle D.

$$\boxed{V_{out} = -\frac{D}{1-D}V_{in}} \tag{2.11}$$

Compared to the *buck* and *boost* converters*, *buck-boost* converter has an output voltage opposite in signe and which can vary continuously from 0 to ∞.

2.2.4 *Flyback* converters

The *flyback* converter is used when it is needed to have a **galvanic isolation** between the input and the outputs. The *flyback* converter is a *buck-boost* converter with the **inductor split to form a transformer**, so that the conversion factor is multiplied by the transformer ratio (n_2/n_1). Moreover, transformer provides an additional advantage : the galvanic isolation (no DC connections) between output and input voltage which allows to referred the output voltage to a desired common mode and sign.

The schematic of a *flyback* converter can be seen in figure 2.10. It is equivalent to that of a *buck-boost* converter but with a transformer instead of inductor. Therefore the operating principle of both converters is very similar :

When the transistor conducts, the primary of the transformer is directly connected to the input voltage source. The primary current and magnetic flux in the transformer increase, storing energy in the transformer. The voltage induced in the secondary winding is negative, so the diode is reverse-biased (*i.e.* blocked). The output capacitor supplies energy to the output load.

When the transistor is blocked, the primary current and magnetic flux drops. The secondary voltage is positive, forward-biasing the diode, allowing current to flow from the transformer. The energy from the transformer core recharges the capacitor and supplies the load.

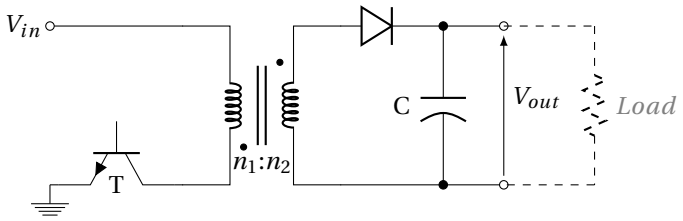


Figure 2.10: *Flyback* topology of an isolated DC/DC converter.

Conversion factor is given by equation 2.12 as a function of the duty cycle D.

$$\boxed{V_{out} = \frac{n_2}{n_1}\frac{D}{1-D}V_{in}} \tag{2.12}$$

*The output voltage ranges for a buck and a boost converter are respectively 0 to V_{in} and V_{in} to ∞.

A DC/DC converter using a transformer as the *flyback* converter is unavoidable if there is a large difference of voltage between V_{in} and V_{out}. Indeed, using *buck*, *boost* or *buck-boost* converter, an output voltage value 100 times smaller (or larger) than the input, require a duty cycle of the order of 0.01 or 0.99 which is not easy to realized (considering that rise and fall time are not 0).

Numerical application : $V_{in} = 300V, V_{out} = 5V$: a *buck* converter require a 0.017 duty cycle (!) while with a *flyback* converter it is possible to stay with a duty cycle close to 50 % by choosing a transformer with a ratio $\frac{n_2}{n_1} = \frac{V_{out}}{V_{in}} \approx 0.017$.

Disadvantage: A transformer, heavy and lossy, is needed.

2.3 Control

A voltage regulator is designed to automatically maintain a constant output voltage level even if V_{in} changes. It require **negative feedback control loops**.

We have see that changing the duty cycle of the switching (*i.e.* Transistor ON/OFF) controls the steady-state output with respect to the input voltage. Then, act on the duty cycle of the transistor driver allows to regulate the output voltage around a constant voltage* even if V_{in}, loads or other parameters change.

2.3.1 Feedback regulation

Feedback principle consist in subtracting† from the "input signal" a fraction of the output one. However, in the case of a DC/DC converter, the "input signal" is more the duty cycle D than V_{in} (Fig. 2.11).

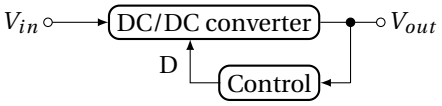


Figure 2.11: Principle of a DC/DC converter feedback voltage regulation. D is the duty cycle of the switching transistor.

2.3.2 Voltage regulation

To do a voltage regulation with a DC/DC converter, a sample of the output voltage is compared to a reference voltage‡ to establish a small error signal V_{err}. This error signal is used to modulate the duty cycle D ($D \propto 1/V_{err}$) of the transistor driver (Fig. 2.21). This modulation of the duty cycle is simply obtained by comparing the error signal with a triangle signal (Fig. 2.13). Duty cycle modulation is also called Pulse Width Modulation (PWM) because if the duty cycle changes, the pulse width also changes.

Regulation is finally obtained because feedback changes the duty cycle from V_{out} then moves the V_{out} to reduce the error signal to zero, thus completing the control loop. The higher the error voltage, the longer the transistor conducts§. V_{err} is derived in the feedback system from the error amplifier that amplifies the difference between the output voltage and the reference voltage :

$$\text{if} \quad \boxed{V_{out} \nearrow \quad V_{err} \searrow \quad D_{PWM} \nearrow \quad D_T \searrow \quad V_{out} \searrow} \tag{2.13}$$

This type of voltage regulation of a DC/DC converter is classified as a voltage-mode controller¶ because the feedback regulates the output voltage. So, if the loop gain is $\gg 1$, the output impedance of the

*by using a proper filtering with a large capacitor.

†Only negative feedback is considered here, because stable operation is required. Moreover, a frequency compensation is needed.

‡The reference voltage could be obtained by using a zener diode D_z biased by the V_{in} through a resistor R.

§considering that the output voltage value is lower than what we want.

¶Another type of control is current-mode control. This method regulates the output current and, with infinite loop gain, the output is a high-impedance source.

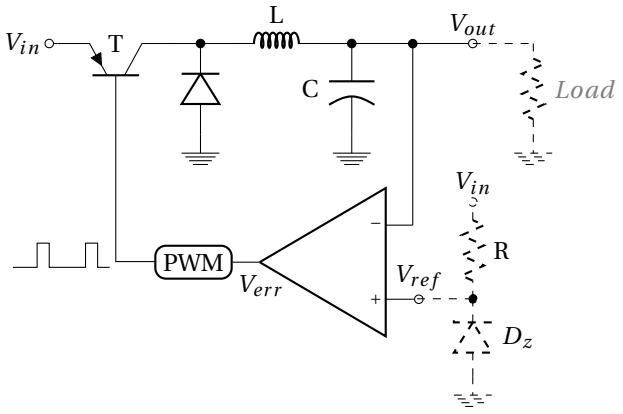


Figure 2.12: Voltage regulation of a *Buck* DC/DC converter by using a Pulse Width Modulator (PWM).

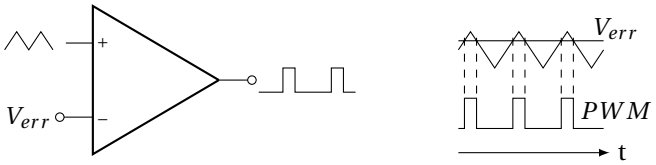


Figure 2.13: Pulse Width Modulator (PWM). Pulse width and duty cycle $D \propto 1/V_{err}$.

regulated voltage converter is 0 Ω. Indeed, output impedance of an ideal voltage source is 0 Ω ; V_{out} is constant what ever the output load (no resistive voltage divider).

Tutorial

2.4 DC/DC converter and duty cycle

A solar panel provides to a satellite a 12V DC power supply refereed to the ground.

1. What types of DC/DC converter allows to generate 5 V? What is the switching duty cycle required?
2. What types of DC/DC converter allows to generate 48 V? Duty cycle?
3. What types of DC/DC converter allows to generate a range of [-5 V : -48 V]? Duty cycles?

2.5 Triangle wave oscillator for PWM

A square signal with a variable duty cycle is required to address transistor of a DC/DC converter. The simplified circuit of a Pulse Width Modulation (PWM) is given in figure 2.14.

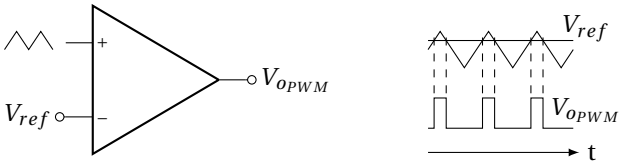


Figure 2.14: Simplified circuit of a Pulse Width Modulation (PWM).

Modulation of the duty cycle is obtain by comparing the V_{ref} reference voltage to a triangle signal. Consider the triangle oscillator given in figure 2.15 with operational amplifiers biased under $\pm V_{bias}$.

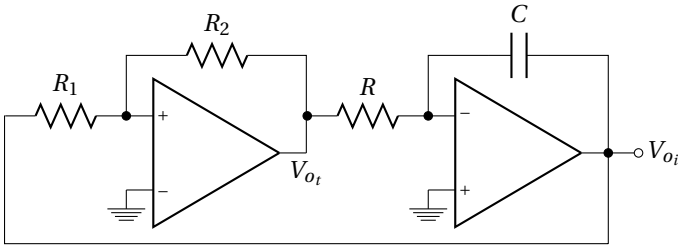


Figure 2.15: Circuit of a triangle wave generator (Schmitt trigger and integrator in a loop).

☞ Due to the positive feedback of the Schmitt trigger: $V_+ \neq V_-$ and $V_{out} = V_{ot} = +$ or $-V_{bias}$ only.

1. Assuming that saturation voltage of operational amplifier = V_{bias}, give a graphic representation (hysteresis curve with arrows) of V_{o_t} as a function of V_{o_i} of the Schmitt trigger alone (Fig. 2.16).
2. Give the wave-form of V_{o_t} and V_{o_i} of the triangle oscillator (Fig. 2.15) as a function of time.
3. Determine the oscillation frequency f_0.
4. Show that f_0 is independent* to the bias while amplitude of the triangle varies with V_{bias}.

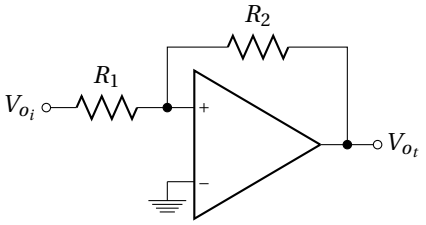


Figure 2.16: Schmitt trigger.

2.6 Preparation of the practical work

2.6.1 Triangle wave oscillator under a single V_{CC} power supply

To bias the circuit of the figure 2.15 under a single $V_{CC} = +20V$ power supply, previous triangle oscillator is modified as figure 2.17 shows.

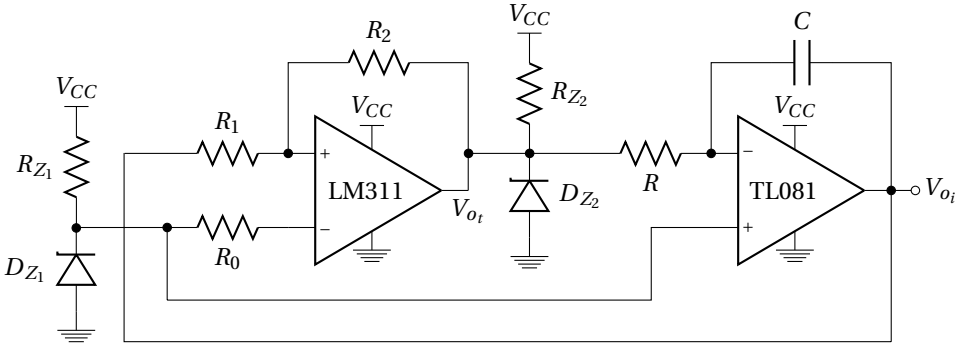


Figure 2.17: Triangle wave generator biased under a single V_{CC} power supply.

A dedicated comparator LM311† is used instead of operational amplifier for the Schmitt trigger. Intermediate 5 V and 10 V voltage references are obtained by using Zener diodes (respectively D_{Z_1} and D_{Z_2}). $R_0 = 1k\Omega$.

1. Give the value of R_{Z_1} and R_{Z_2} of the two 5V and 10V Zener diodes to limit current at 10 mA in this two diodes.
2. Determine the value of R, C, R_1 and R_2 to have a 20 kHz oscillation frequency with a triangle amplitude of $5V_{pp}$. Current is limited to about 500 μA in R and R_2.
3. Check that the slew rate of the TL081 operational amplifier is compatible with the triangle wave slope.

*independent common-mode frequency
†The LM311 has an open collector → D_{Z_2} fix the maximum output voltage.

2.6.2 Comparator

Circuit of the comparator using the triangle signal (V_{o_i}) is given in figure 2.18. A voltage divider bridge is proposed to test the operation of the comparator and of the PWM.

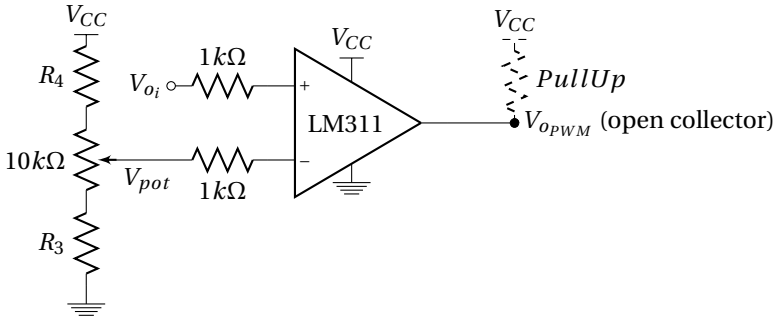


Figure 2.18: Pulse Width Modulation generator using triangle signal and adjustable reference voltage.

1. Give the value of R_3 and R_4 to have V_{pot} which allows to describe the overall amplitude of the V_{o_i} signal, at the output of the potentiometer (at the slider).
2. Give the link between the duty cycle of $V_{o_{PWM}}$ and the slider voltage value V_{pot}.

2.6.3 Switching transistor

Pulse Width Modulation signal is applied to a PNP transistor BDX54 as shown in figure 2.19.

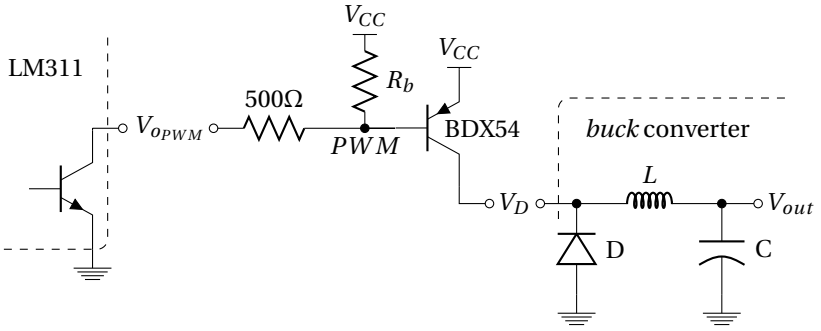


Figure 2.19: Switch transistor for *buck* converter. V_D is connected to the cathode of the diode of the buck converter.

1. Explain the operation of the transistor BDX54 if PWM signal is V_{CC} and ground.

Consider the necessity of the R_b resistor. Indeed, switching circuit can not operate well without this resistor because LM311 are "open" collector output (Emitter is connected to the ground ; see datasheet) which not fix by itself the output voltage*.

Without R_b, transistor conducts well (saturation region) for a $0V$ LM311 output, but does not block for a high impedance LM311 output (or only after a long time thanks to leakages). So, R_b is crucial to avoid a permanent transistor saturation and for a good operation of the transistor on switching-mode with good control of the duty-cycle value.

R_b value is then chosen to be the smallest to allow a fast transition between saturation and cut-off mode of the transistor (see datasheet of the transistor BDX54).

*Low LM311 output voltage = $0V$, but high "output level" correspond only to a high impedance state which not set the voltage value.

2. Give the minimum value of R_b which still allows the transistor saturation.

2.6.4 DC/DC *buck* converter

Circuit of the DC/DC *buck* converter without control is given in figure 2.20.

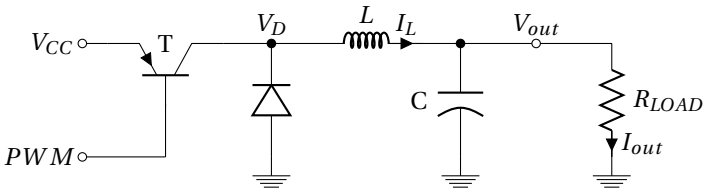


Figure 2.20: DC/DC *Buck* converter using the PWM as a driver of the transistor.

L = 1 mH and C = 1000 μF

1. Give a graphic representation of I_L, V_D, V_{out} and $V_L = V_D - V_{out}$ in the continues case (*i.e.* I_L is never null).
2. Give the expression of the average value of the output voltage $\overline{V_{out}}$ as a function of V_{CC} and the duty cycle D.
3. Deduce the expression of $\overline{V_{out}}$ as a function of V_{CC} and ΔV_{pot} for a V_{pot} which go from 2.5 V to 7.5 V.

2.6.5 Voltage regulation

Figure 2.21 shows a part of the regulation circuit, for an open loop studies.

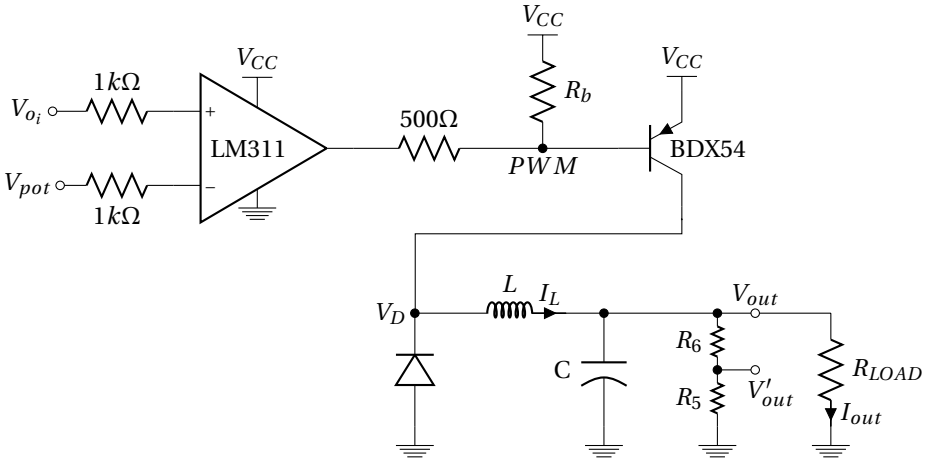


Figure 2.21: Open loop regulation of a DC/DC *Buck* converter.

A $5V$ voltage reference (D_{Z_1} of the triangle generator) will be used for the regulation of the output voltage of the DC/DC *buck* converter at around $V_{out} = 10V$.

1. Compute the maximum power dissipation in the 500 Ω. What kind of resistor is required.
2. Found values ($\gg R_{LOAD}$) of R_5 and R_6 to have $V'_{out} = 5V$

A transfer function of the open loop $\frac{V'_{out}}{V_{pot}}$ is given in figure 2.22.

This open loop gain is measured around a $10V$ output average value, by applying a 1 V sine wave in addition to a static value in V_{pot}.

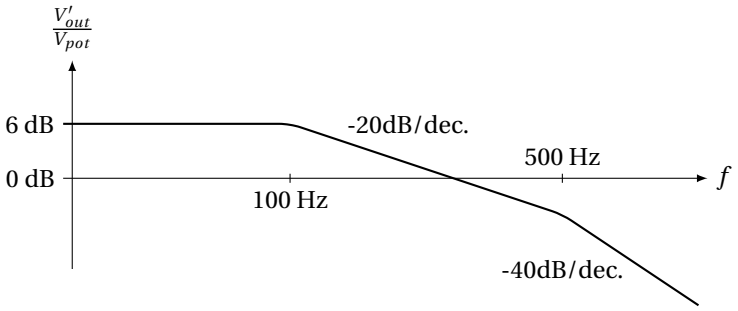


Figure 2.22: Transfer function of the open loop gain of $\frac{V'_{out}}{V_{pot}}$.

3. Give the transfer function $\frac{V'_{out}}{V_{o_i}}$ if the loop is closed ?
4. Show that a proportional (P*) control could increase static performances.
5. What is the drawback of this correction on the loop stability ?

An operational amplifier LM158, could be used to realized both comparator and proportional controller (Fig. 2.23).

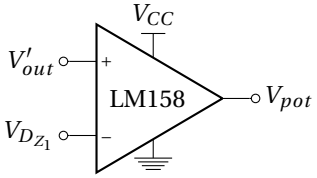


Figure 2.23: Comparator proportional with a LM158.

You will obtaine a high open loop gain with a negative feedback as shown in figure 2.24.

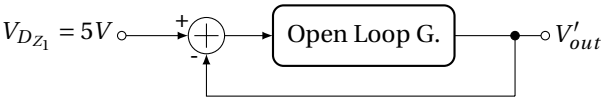


Figure 2.24: Block diagram of the control.

6. Give an asymptotic representation of the new open loop gain using P = 10 control.
7. What is the new performances of the system ? Is it stable ?
8. What kind of control (P, PI, PD) allows to increase static performance without instability ?

We finally prefer the use of a PI control given in figure 2.25.

9. Give the small signal transfer function $\frac{V_{pot}}{V'_{out}}$ with $V_{D_{Z1}} = DC$.
10. Give a value of C_0 which increases static performances while keep stable operation. Illustrate by a graphic representation of the open loop gain this last control.

*As the P of a Proportional, Integral and Derivative (PID) controller of a generic control loop feedback

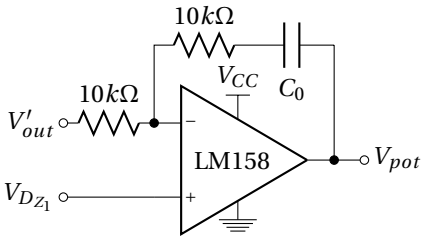


Figure 2.25: Comparateur proportional/integrator with a LM158.

Lab work

The purpose of this practical work is to build a DC/DC *buck* step-down converter, 20 V to 10 V on a 30 Ω load resistor and with voltage regulation.

Preliminary settings

Set the current limitation of the 20 V power supply at a maximum current of 600 mA (O.C.P = 600 mA ; O.V.P = 21 V).

2.7 Pulse Width Modulation (PWM)

Build on the solder-less breadboard the three parts of the Pulse Width Modulation given in figure 2.26.

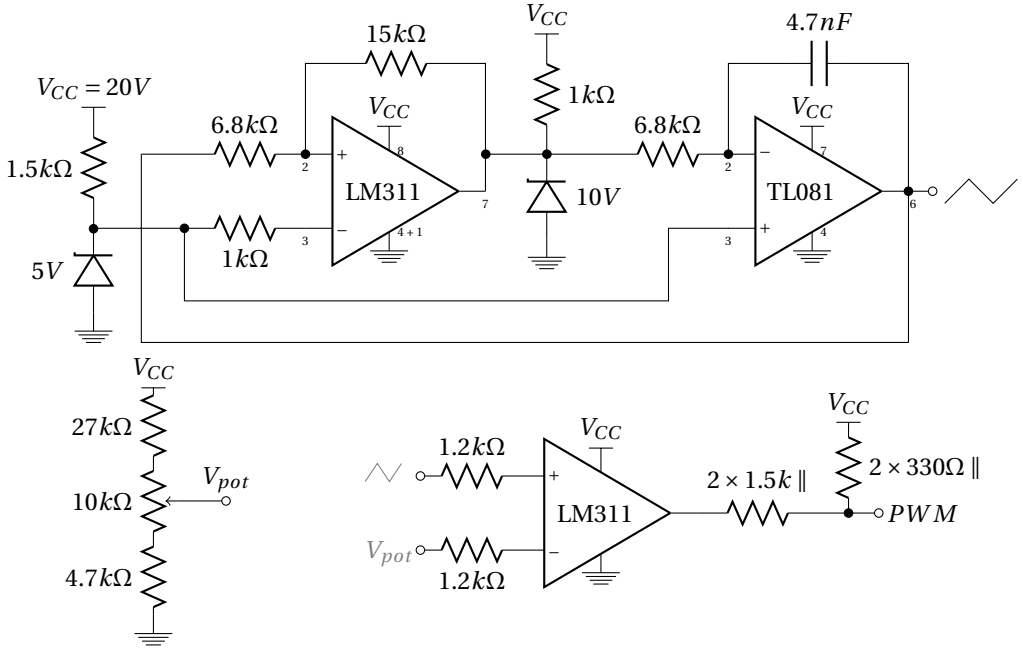


Figure 2.26: Building blocks needed for the Pulse Width Modulation generator biased under a single $V_{CC} = 20V$ power supply.

1. Bias the triangle generator of the figure 2.26 under 20 V and plot the triangle signal obtained.
2. Check that V_{pot} give well a voltage from 2.5 V to 7.5 V. Give the V_{pot} extreme values obtained.
3. Connect the triangle signal to the non-inverting input of the comparator, and V_{pot} to the inverting one. Look the PWM signal and check that the duty-cycle D evolves well with V_{pot}. Measure the V_{pot} corresponding to D=0 and D=1.

2.8 Transistor driver

Connect the PWM signal to the base of the Darlington PNP transistor BDX54 (Fig. 2.27) loaded by a 30 Ω resistor. Be careful to this load resistance ; ⚠ it can be VERY hot ⚠

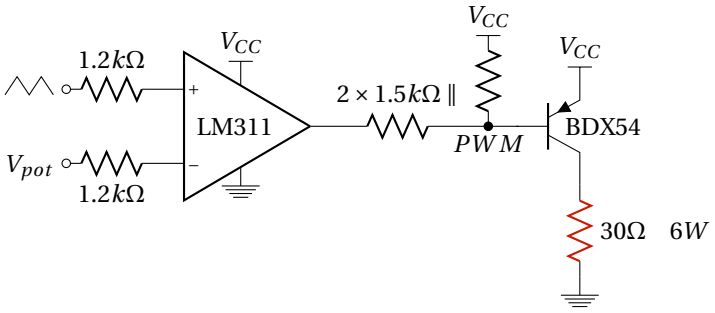


Figure 2.27: Transistor driver and loading.

1. Look the output voltage across R_{LOAD} with and without R_b. Draw waveforms of the PWM signal and of the BDX54 collector voltage in the two cases.
2. What is the duty-cycle obtained with and without R_b.

2.9 Waveform signals in a *buck* converter

Build the DC/DC *Buck* step-down converter as figure 2.28 with L = 1 mH, C = 1000 μF and R_{LOAD} = 30 Ω. Set the potentiometer to have $V_{out} = 10V$.

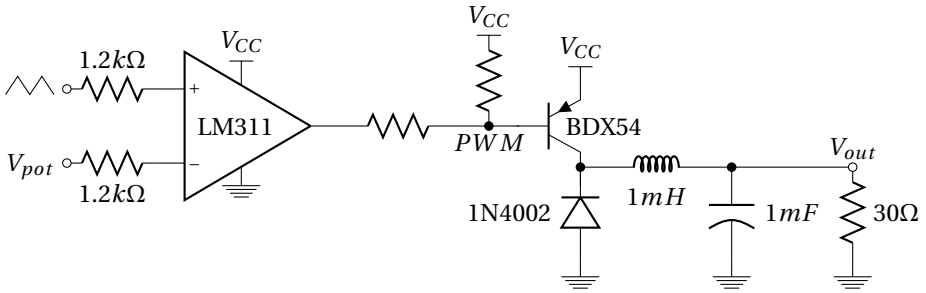


Figure 2.28: DC/DC *Buck* converter with transistor driver.

1. Add a 1 Ω resistor in series with L to measure the current I_L. Give a graphic representation of the measured ΔI_L and ΔV_{out}.
2. Compare ΔI_L with $\frac{V_{out}}{L} T_{OFF}$.

2.10 Voltage regulation

We are now interested in the open loop $\frac{V'_{out}}{V_{pot}}$ of a control feedback (Fig. 2.29). Choose $R_5 = R_6$ large as compared to R_{LOAD}. Apply an offset (DC voltage $\approx 5V$) in addition to an input 1V sine wave instead of V_{pot} so as to have $\overline{V_{out}} = 10$ V.

1. Measure the V'_{out} ripple amplitude as a function of the frequency. Give the transfer function V'_{out}/V_{pot}. Compare with tutorial.

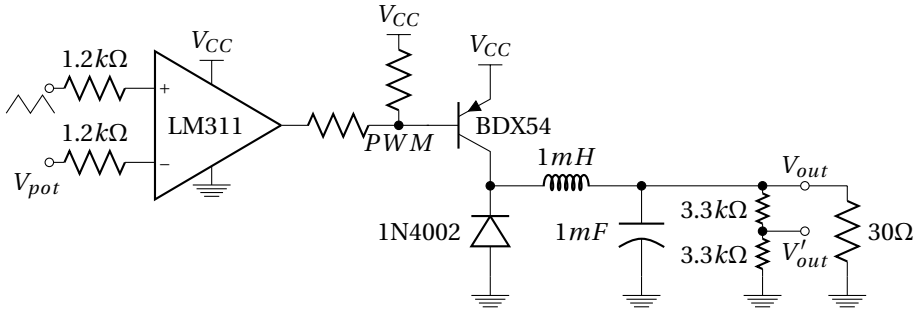


Figure 2.29: DC/DC *Buck* converter with open loop control feedback.

2. Use the control given in figure 2.30 to close the control loop. Slightly change the V_{CC} voltage value around 20 V to check that the output voltage is well regulated at 10 V whatever V_{CC}. .

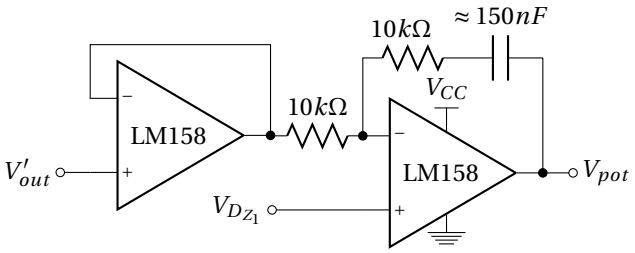


Figure 2.30: Proportional/integrator comparator with a LM158.

☞ Disassemble and clean

Part III

Phase Locked Loop

3 Phase Locked Loop

3.1 Introduction

THE Phase Locked Loop (PLL) plays an important role in modern electronic and particularly for space communications. Indeed, PLL is a crucial part of modulator, demodulator or synchronization systems. As example of space application (Fig. 3.1), PLL is particularly essential to estimate the instantaneous phase of a received signal, such as carrier tracking from Global Positioning System (GPS) satellites.

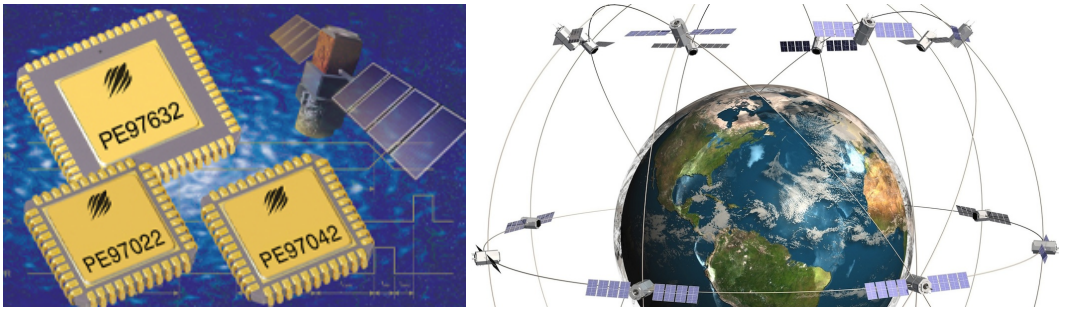


Figure 3.1: PLLs used for space applications (`Peregrine Semiconductor`); GPS constellation around the Earth.

PLL allows to **extract signals from noisy transmission channels**. Indeed, communications between satellites and ground stations are usually buried in atmospheric noise or some type of interferences (frequency selective fading* or doppler shift†) which one manage by a PLL.

PLL circuits can also be used to distribute clock signal, or set up as frequency multipliers or dividers for frequency synthesis.

3.2 Description

PLL is a **feedback electronic circuit** (control system) as shown in figure 3.2. It includs an **oscillator** which is constantly adjusted in order to match the **instantaneous phase** (therefore the frequency) of the PLL input signal. The oscillator is a **Voltage Controlled Oscillator** (VCO)‡ whose frequency varies with an **"error" signal** $\epsilon \approx V_{VCO}$. This "quasi-DC" voltage come from a **phase detector** (ϕ comp.). It is proportional to the phase difference between the input signal which varies in frequency as $f_{in}(t)$ and

*Frequency selective fading : Radio signal arrives at the receiver by two different paths.

†Doppler shift : Shift in frequency for a receiver moving relative to the emitter

‡A VCO is an electronic oscillator (output) designed to be controlled in oscillation frequency by a voltage input. The frequency of oscillation is varied by the applied DC voltage.

VCO output frequency $f_{out}(t)$. Frequency noises (jitter*) are suppressed after phase comparison, by adding a filter before the VCO. Thus, PLL recovers, at the output, the original signal from a noisy version of the received signal.

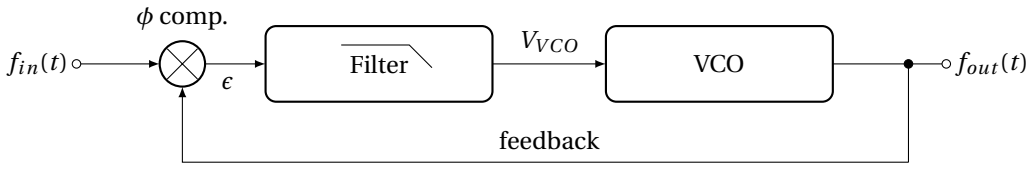


Figure 3.2: Block diagram of a PLL.

Phase comparison can also be made after a division of the VCO frequency, which allows to have a PLL output signal with a larger frequency. This technique is used for frequency synthesis.

☞ A Phase Locked Loop is thus mainly composed by two key ingredients :

- **Phase detector/comparator more or less associated to a filter**
- **Voltage Controlled Oscillator (VCO)**

3.2.1 Phase detector/comparator

One key element of the PLL, is the phase comparator. A phase comparator is a frequency mixer, analog multiplier or logic circuit that generates a **voltage signal whose mean value is proportional to the difference in phase** between two input signals.

Analog phase detector

Mixing (or product) of two sine waves at similar frequencies as f_{in} and f_{out} gives, in frequency domain, a signal at the sum and at the difference of the two input signal frequencies†. The high frequency at $f_{in}+f_{out}$ is removed by filtering‡. The low frequency (static if $f_{in}=f_{out}$) could be expressed as a function of phase difference $\Delta\phi$ (equation 3.1).

$$\begin{aligned} &\sin\left(2\pi f_{in}t+\phi_{in}\right)\times\sin\left(2\pi f_{out}t+\phi_{out}\right) \\ \propto\ &\underbrace{\cos\left(\Delta\phi\right)}_{\text{static}}-\underbrace{\cos\left(2\pi(f_{in}+f_{out})t+\phi_{in}+\phi_{out}\right)}_{\text{filtered signal}} \end{aligned} \tag{3.1}$$

So multiplication allows to detect phase difference between two sine waves. This is why phase comparator is currently represented by the symbol $\otimes$ as in figure 3.2.

A circuit diagram of an analog multiplier (mixer) is given in figure 3.3. This is a simple analog circuit playing the role of phase detector§ using a "diode ring" and transformers having middle point of the secondary winding.

Digital phase detector

Phase locked loop device as the popular CD4046 integrated circuit (see *Datasheet* in Appendix I) includes two kind of digital phase comparators :

- **Type I** phase comparator is designed to be driven by analog signals or square-wave digital signals and provides an output pulse at twice the input frequency. this waveform must be filtered before to drive the VCO (the average voltage is proportional to the phase difference).

*The jitter is an undesired deviation from time periodicty of an assumed periodic signal. PLL is a jitter suppressor.

†$2\sin a\sin b=\cos(a-b)-\cos(a+b) \quad\Rightarrow\quad 2\sin(\propto f_{in})\sin(\propto f_{out})=\cos[\propto(f_{in}-f_{out})]-\cos[\propto(f_{in}+f_{out})]$

‡This is why the phase comparator is systematically associated to a filter/integrator.

§The IF (Intermediate Frequency) varies as the cosine of the phase different between the RF (Radio-Frequency) and LO (Local Oscillator) inputs. 0 V correspond to a phase difference = 0; min and max voltages are therefore linked to a phase = π; at multiples of 2π.

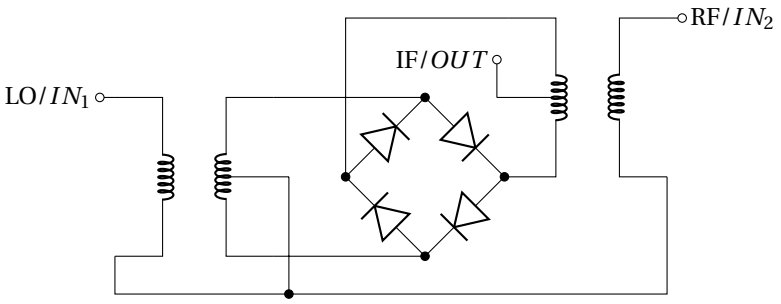


Figure 3.3: Diode ring (double balanced) multiplier used as an analog phase detector. LO and RF can be used as inputs of the phase comparator. IF provides a voltage following the phase difference of the two inputs.

- **Type II** phase comparator is sensitive only to the relative timing of the edges of the inputs. In steady state (both signals are at the same frequency), it produces a constant output voltage proportional to the phase difference. This output will tend not to produce ripple in the control voltage of the VCO.

Type I phase detector : XOR The simplest phase comparator is the eXclusive OR (XOR) gate. A XOR gate is a digital logic gate which compute the binary addition* which is symbolized by $\oplus$. XOR truth table is shown in figure 3.1.

A	B	A $\oplus$ B
0	0	0
0	1	1
1	0	1
1	1	0

Table 3.1: XOR truth table.

Type I comparator will be appropriate for square waves (v_1 and v_2 in figure 3.4) but could also be used with sine wave inputs. Its operation is highly dependent on the duty cycle of the input signals and is not really usable for duty cycle too different from $\frac{1}{2}$.

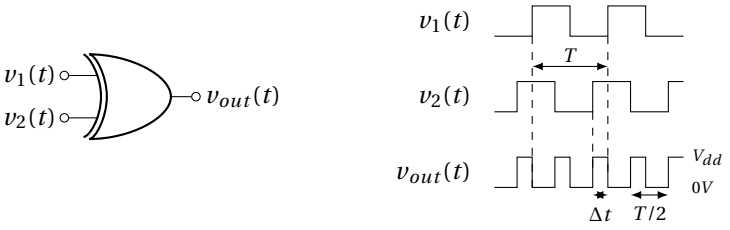


Figure 3.4: XOR phase comparator.

The phase difference between v_1 and v_2 could be expressed as a function of the pulse width Δt and the frequency f as expression 3.2.

$$\Delta\phi = 2\pi\frac{\Delta t}{T} = 2\pi f \Delta t \tag{3.2}$$

*Binary addition ≡ addition modulo 2.

For a duty cycle = $\frac{1}{2}$, XOR provides pulse train with twice the frequency of v_1 and v_2. This periodic square wave signal v_{out} has a duty cycle ($D_{v_{out}} = \frac{\Delta t}{T/2} = 2f\Delta t$) given by expression 3.3, function of input phase difference $\Delta\phi$.

$$D_{v_{out}} = \frac{\Delta\phi}{\pi} \tag{3.3}$$

Then, the output of the XOR gate can be expressed as a static value $\overline{V_{out}}$ and harmonics ($\frac{2}{T}$ frequency at least) as a Fourier series : see the equation 3.4 with v_n and ϕ_n the amplitude and the phase of the n^{th} harmonic at the frequency $\frac{2n}{T}$.

$$v_{out} = \underbrace{\overline{V_{out}}}_{static} + \underbrace{\sum_{n=1}^{n\to\infty} v_n \sin\left(2\pi\frac{2n}{T}t - \phi_n\right)}_{harmonics} \tag{3.4}$$

This pulse train is averaged* before the VCO to keep only the static signal.
The averaging value of the XOR output could be linked to the pulse width as expressed on 3.5.

$$\overline{V_{out}} = D_{v_{out}} V_{dd} = \frac{2\Delta t}{T} V_{dd} \tag{3.5}$$

Finally, we could obtain the information about the phase difference $\Delta\phi$ from the XOR output averaging value using the expression 3.6. This expression allows to show the phase comparator gain K_p.

$$\overline{V_{out}} = \frac{\Delta\phi}{\pi} V_{dd} = K_p \Delta\phi \tag{3.6}$$

The characteristics of an XOR phase comparator is represented in figure 3.5. It is periodic in $\Delta\phi$ with period of 2π. The range $0 \leq \Delta\phi \leq \pi$ is the range where the PLL can operate in the locked condition (linear regime).

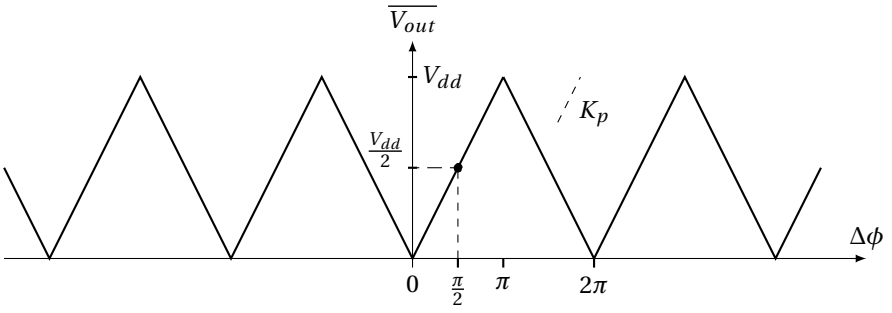


Figure 3.5: Periodic characteristic of an XOR phase comparator and a typical operating point. The slope K_p is the gain of the comparator.

The transfer function of this phase comparator on this linear part is given by expression 3.7. K_p is called the **gain of the phase detector**.

$$\boxed{\frac{\overline{V_{out}}}{\Delta\phi} = K_p = \frac{V_{dd}}{\pi}\Big|_{0\leq\Delta\phi\leq\pi} \quad \text{[V/Rad]}} \tag{3.7}$$

When PLL is in lock condition with this type of comparator, the steady-state phase difference at the inputs is usually near $\frac{\pi}{2}$ (depend on the VCO) - often in the middle of the phase comparator (linear regime).

So, this kind of phase comparator generates always an output "digital" signal in the PLL loop. Therefore, despite low-pass filter, it always remain residual ripples, and consequent periodic phase variations at two times the frequency signals.

*The loop filter acts as a low pass filter (or integrator), smoothing this full-swing logic-output signal.

Type II phase detector : charge pump A scheme of a type II phase comparator is given in figure 3.6.

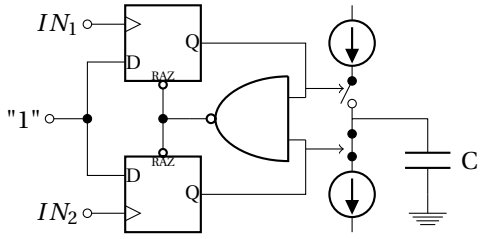


Figure 3.6: Dual D-Type phase detector : a type II phase detector.

By contrast to the type I comparator, the type II phase detector generates output pulses **only when there is a phase error** between the input and the VCO signal and follow the characteristic illustrated on figure 3.6 :

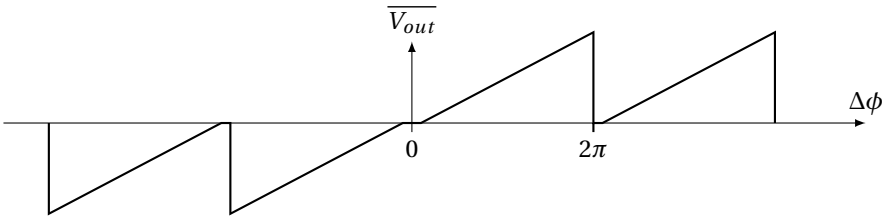


Figure 3.7: Periodic characteristic of a Type II charge pump detector.

- **If the two input are in phase :** The phase detector looks like an open circuit and the loop filter acts as a voltage-storage device, holding the voltage that gives the VCO frequency.
- **If the input signal moves away in frequency :** The phase detector generates a train of short pulses*, charging the capacitor of the filter to the new voltage needed to keep the VCO locked.

So, the output pulses disappear entirely when the two signals are in lock†. This means that there is no ripple in the output as compared to type I phase detector.

3.2.2 Voltage Control Oscillator - VCO

The other key ingredient of the PLL, is the VCO. It exist two different types of controlled oscillators :

- Resonant/Harmonic oscillators ($\geq$ 50 MHz)
- Relaxation oscillators ($\leq$ 50 MHz)

For microwave applications, resonant oscillators implemented with devices as LC tank circuit is used. C value is adjusted (tuning) thanks to a varactor diode.

However, we will concentrate on non-microwave applications, and thus on the relaxation oscillators more easily implementable on integrated circuit (similar to the triangle oscillator of the DC/DC part). This is typically the VCO that we can find in the CD4046 PLL integrated circuit (see data sheet). V_{VCO} controls the **charging and discharging** currents through an external‡ capacitor C, and therefore determines the time needed to charge and discharge the capacitor to a pre-determined **threshold level**. As a result, the frequency f_{VCO} changes as a function of V_{VCO}.

*The short pulses contain very little energy and are easy to filter out of the VCO control voltage. This results in low ripples.

†A charge pump phase detector must always have a "dead frequency band" where the phases of inputs are close enough leading to no phase error in the comparator phase. So, charge pump introduce necessarily a significant peak-to-peak jitter, because of drift within the dead frequency band.

‡not implemented on the CD4046 to allow tuning of the f_{VCO_0} center frequency.

If V_{VCO} evolves, a linear VCO transfer function can be expressed as equation 3.8.

$$\begin{aligned} \frac{f_{max}-f_{min}}{V_{max}-V_{min}} &= K_0 \quad [\text{Hz/V}] \\ &= \frac{\mathrm{d}f_{VCO}}{\mathrm{d}V_{VCO}} \quad = \frac{f_{VCO}}{V_{dd}/2} \quad \text{if no "offset" } ie \quad f_{min}=0 \quad \text{and} \quad V_{min}=0 \end{aligned} \tag{3.8}$$

In practice V_{max} is limited by V_{DD} and V_{min} by $0V$ (or V_{SS}). Assuming a linear response as in figure 3.8, f_{max} and f_{min} are adjusted and therefore fix the gain K_0.

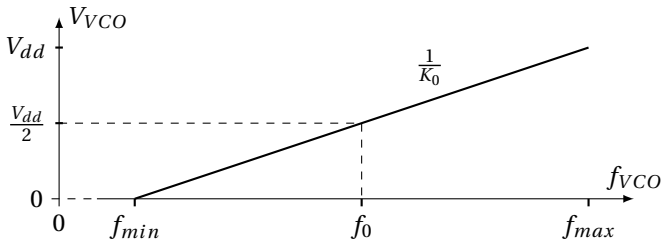


Figure 3.8: VCO characteristic : V_{VCO} as a function of f_{VCO}.

The VCO transfer function can also be expressed using the angular frequency ω_{VCO} as eq. 3.9.

$$\boxed{\frac{\omega_{VCO}}{V_{VCO}} = 2\pi K_0 = K_v \quad [\text{Rad/(V.s)}]} \tag{3.9}$$

⚠ *The VCO gain is usually expressed as a radian frequency per voltage; so its units are rad/(V.s) even if the "rad" is often omitted.*

However, for a **P**LL, this is the **phase** instead of the frequency which is interesting. It is then more useful to express the phase output of the VCO :

$$\int \omega_{VCO}(t)\mathrm{d}t = \phi_{VCO}(t) \quad \rightarrow \quad \frac{\omega_{VCO}(s)}{s} = \phi_{VCO}(s) \tag{3.10}$$

Then the transfer function between the phase and the input voltage of the VCO is finally given by expression 3.11

$$\frac{\phi_{VCO}(s)}{V_{VCO}(s)} = \frac{K_v}{s}[Rad/V] \tag{3.11}$$

3.3 Frequency range

Operating frequency range of a PLL is graphically represented in figure 3.9. Two main frequency ranges appear :

- Lock range
- Capture range

3.3.1 Lock range $2\Delta f_L$

The Lock range (also called Hold range) is the frequency range in which a PLL is able to stay locked. It correspond to a "**static** stable frequency range"; this means that the PLL remains locked if the input signal is a **fixed frequency** signal comprised in this range.

The Lock range is mainly defined by the VCO range.

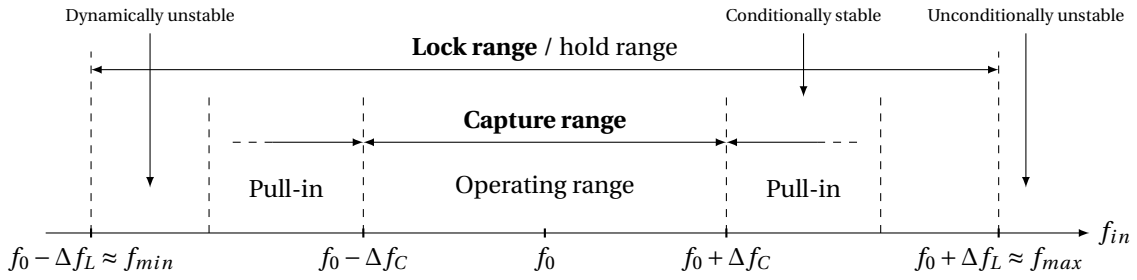


Figure 3.9: Scope of the 2 main frequency ranges of a PLL : Lock (or Hold) range and Capture range (more or less defines because of "pull-in" effect). f_0 correspond to the VCO center frequency.

Figure 3.5 shows that when the phase comparator is used on a PLL, the phase difference $\Delta\phi$ need to be small enough to stay on a linear regime. So, VCO is used to operate around a center frequency $f_{VCO_0} = f_0$ and around $V_{VCO_0} = \frac{V_{dd}}{2}$* as it is represented in figure 3.8. Thus, $\Delta\phi_{max} = \pi$ around this operating point (eq. 3.12 and Fig. 3.5).

$$0 \leq \Delta\phi \leq \pi \tag{3.12}$$

Knowing that $\Delta\phi$ must be included in $[0;\pi]$ range, we can expressed the maximum range in frequency at the output of the VCO as equation 3.13 (from Fig. 3.8 → $f_{max} - f_{min} = K_0 V_{dd}$ and Fig. 3.5 → $V_{dd} = \pi K_p$).

$$\underbrace{f_{max} - f_{min}}_{\text{Lock range}} = \pi K_0 K_p = \frac{K_v K_p}{2} \tag{3.13}$$

From this expression, lock range $2\Delta f_L = f_{max} - f_{min}$ is defined as equation 3.14.

$$\boxed{2\Delta f_L = \frac{K_v K_p}{2}} \tag{3.14}$$

If f_{in} exceeds f_{max} (or if f_{in} becomes smaller than f_{min}), the PLL fails to keep $f_{VCO} = f_{in}$, and the PLL becomes unlocked. When the PLL is unlocked, the VCO generally oscillates at the frequency f_0 (the **"free-running"** of the VCO). The lock can be established again if the incoming signal frequency f_{in} gets close enough to f_0 *i.e.* as close as the Capture range.

The VCO output frequency f_{VCO} can be plotted (Fig. 3.10) as a function of the input PLL frequency f_{in}.

This characteristic simply shows that $f_{VCO} = f_{in}$ in the locked condition, and that $f_{VCO} = f_0$ when the PLL is unlocked. A hysteresis is observed if the Lock range is larger than the Capture range.

3.3.2 Capture range $2\Delta f_C$

The capture range is the frequency range where the PLL is able to "quickly" **lock-in, starting from unlocked condition**. Indeed, in most practical applications, it is desirable that the locked state is obtained within a short time period. So, the capture range point out that the PLL can become locked within "one single-beat". This is called a **lock-in process**. Beyond this frequency range, a **pull-in process** also allows the PLL to lock, but slowly. There is obviously a blurred boundary (Fig. 3.9) between Capture range and pull-in range, but we can notice that:

- Lock-in process is much faster than pull-in process
- Capture range is smaller than pull-in range

*In this operating point, the two compared signals are in quadrature.

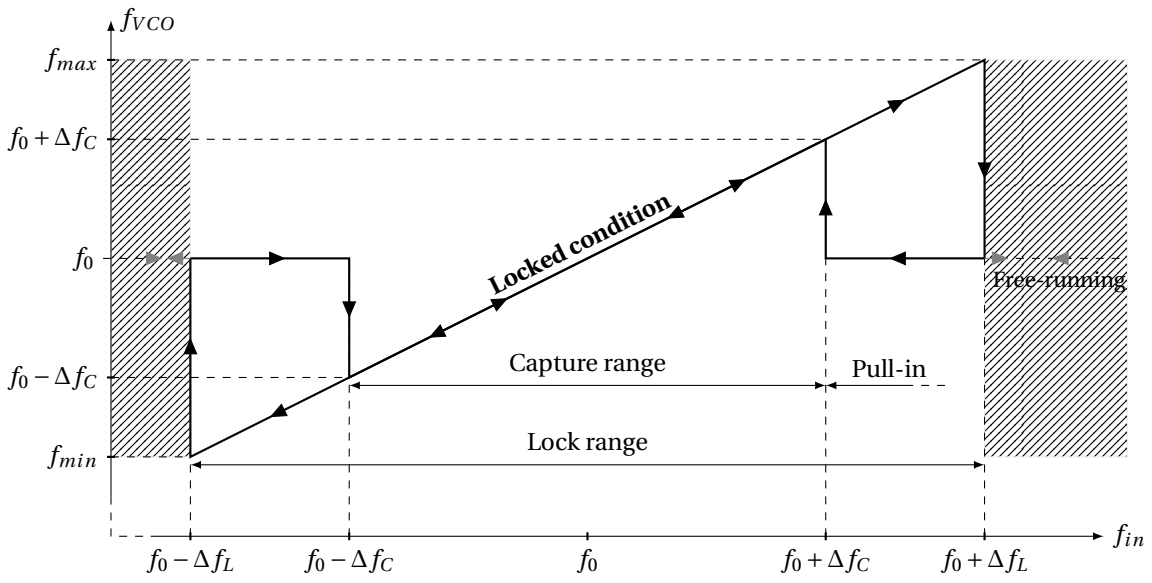


Figure 3.10: Hysteretic PLL characteristic.

Capture range refers to the dynamic behavior of the PLL loop. So $2\Delta f_C$ depends on the loop bandwidth. In the case of a single pole filter and a $Q < 1$, the Capture range is simply equal to the Lock range: $2\Delta f_C = 2\Delta f_L$.

☞ Capture range is not necessarily centered on f_0.

3.4 Frequency response

For a small phase difference ($\sin\phi \approx \phi$) between PLL input signal and VCO output, PLL can be accurately described by a linear model expressed as regard to the phase instead of frequency. Block diagram of this linear model is given in figure 3.11. $\frac{K_v}{s}$ is the gain of the VCO (small signal analysis) expressed as equation 3.11 as regard to the phase. The loop filter plays a crucial role in the frequency response of the PLL. Its transfer function is called $H_{filter}(s)$, or more simply $H(s)$.

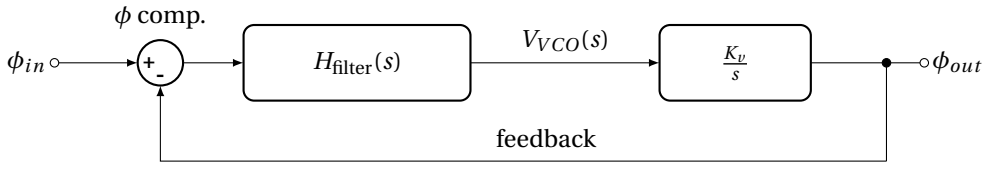


Figure 3.11: Block diagram of PLL on phase domain.

The PLL response can be written as 3.15.

$$\frac{\phi_{out}}{\phi_{in}} = \frac{\text{forward gain}}{1 + \text{loop gain}} = \frac{K_p \frac{K_v}{s} H(s)}{1 + K_p \frac{K_v}{s} H(s)} \tag{3.15}$$

The transfer function $H(s)$ of the filter averages the output of the phase comparator and suppresses noise of the input signal.

3.4.1 One pole loop filter

For a simple first order RC filter (Fig. 3.12), the H(s) transfer function is given by expression 3.16

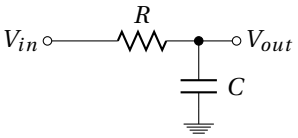


Figure 3.12: One pole filter used as PLL loop filter.

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{1}{1+RCs} \tag{3.16}$$

Using this one pole filter, the PLL response is expressed as 3.17.

$$\frac{\phi_{out}}{\phi_{in}} = \frac{1}{1+\frac{1}{K_pK_v}s+\frac{RC}{K_pK_v}s^2} \tag{3.17}$$

Denominator could be rewritten as expression 3.18 to show the natural angular frequency $\omega_n = 2\pi f_n$ and the quality factor Q (damping factor $\zeta = \frac{1}{2Q}$) of the PLL response.

$$1+\frac{1}{Q}\frac{s}{\omega_n}+\frac{s^2}{\omega_n^2} \quad \begin{cases} \omega_n &= \sqrt{\frac{K_pK_v}{RC}} \\ Q &= \sqrt{K_pK_vRC} \end{cases} \tag{3.18}$$

The natural frequency of the PLL gives information about the response time of the locked system. Moreover, the quality factor inform us to overshoot and ringing. Ideally, the natural frequency should be high and the quality factor should be near unity (critical damping). But, with a single pole filter, it is not possible to control the loop frequency and quality factor independently.

Assuming a critical damping ($Q = 0.5$ *i.e.* $\zeta = 1$) for stable PLL operation : $RC = \frac{1}{4K_pK_v} \rightarrow \omega_n = 2K_pK_v$.

☞ In other words, **the ability of the PLL to filter the input "frequency noise" is limited by the stable condition of the loop**.

3.4.2 One pole - one zero loop filter (like PID)

A One pole - one zero filter allows to adjust independently the bandwidth of the PLL response and the damping factor. It is composed of two resistors and one capacitor (Fig. 3.13). The transfer function of this filter is given in expression 3.19 and plot in figure 3.14. It is characterized by two time constants : τ_1 and τ_2.

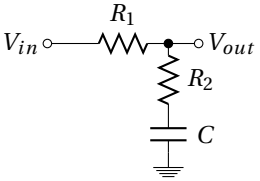


Figure 3.13: One pole - one zero filter used as PLL loop filter.

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{1+\tau_2 s}{1+\tau_1 s} \quad \begin{cases} \tau_1 &= (R_1+R_2)C \\ \tau_2 &= R_2C \end{cases} \tag{3.19}$$

Using this one pole - one zero filter, the PLL response is now expressed as 3.20.

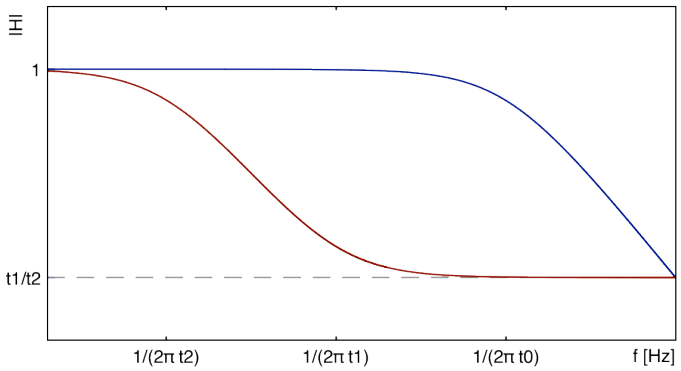


Figure 3.14: Amplitude Bode plot of a one pole (RC=t0) and a one pole - one zero ($(R_1+R_2)C$=t1 and R_2C=t2) filter .

$$\begin{aligned}\frac{\phi_{out}}{\phi_{in}} &= \frac{K_p \frac{K_v}{s}\frac{1+\tau_2 s}{1+\tau_1 s}}{1+K_p \frac{K_v}{s}\frac{1+\tau_2 s}{1+\tau_1 s}} \\ &= \frac{1}{1+\frac{s}{K_p K_v}\frac{1+\tau_1 s}{1+\tau_2 s}} \\ &= \frac{1+\tau_2 s}{1+\frac{1+K_p K_v \tau_2}{K_p K_v}s+\frac{\tau_1}{K_p K_v}s^2}\end{aligned} \tag{3.20}$$

Denominator could be rewrite as expression 3.21.

$$1+\frac{1}{Q}\frac{s}{\omega_n}+\frac{s^2}{\omega_n^2} \quad \begin{cases} \omega_n &= \sqrt{\frac{K_p K_v}{\tau_1}} \\ Q^{-1} &= \frac{1}{\omega_n \tau_1}+\omega_n \tau_2 \end{cases} \tag{3.21}$$

The loop filter time constantes (equation 3.22) can now be calculated independently for a given natural frequency f_n and damping factor ζ.

$$\begin{cases} \tau_1 &= \frac{K_p K_v}{\omega_n^2} \\ \tau_2 &= \frac{1}{Q\omega_n}-\frac{1}{K_p K_v} \end{cases} \tag{3.22}$$

3.5 Frequency Shift Keying (FSK) demodulation

We will studie the use of a PLL in the case of FSK demodulation. Frequency-shift keying is used for data transfer in space communications. It is a frequency modulation scheme in which digital information is transmitted through two different frequencies : *mark* frequency the "1" (binary ones) and space frequency the "0" (binary zeros). The time domain of a FSK modulation is illustrated in the figures 3.15.

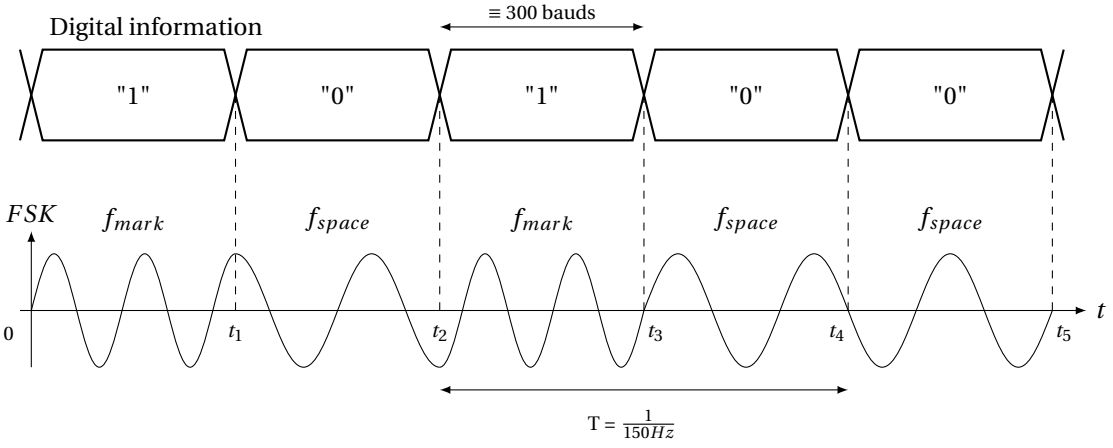


Figure 3.15: Digital information FSK modulated.

Specification of the FSK modulation studied in this tutorial

- f_{mark} = 2200 Hz ≡ "1"
- f_{space} = 2000 Hz ≡ "0"
- bit rate = 300 bit/s *

demodulation To do the FSK demodulation, a specific voltage value is associated to each frequency in order to recovery bit digital data. This is performed by using a PLL (Fig. 3.16) characterized by following specifications :

*In telecommunications the symbol-rate is also named *baud* [Bd]; for binary code 1 Bd = 1 bit/s. In the case of the figure 3.15, the bit rate is equal to $\frac{1}{t_1} = \frac{1}{t_2-t_1} = \frac{1}{t_3-t_2}$ ...

- PLL continuously locked
- Capture range * $\Delta 2 f_C \geq 2(f_{mark} - f_{space})$
- feedback slightly underdamped : $\zeta = 0.5$ †

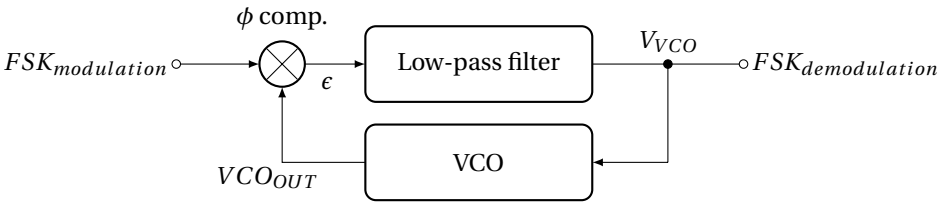


Figure 3.16: FSK demodulation using PLL.

- Give the shape of the V_{VCO} of the figure 3.16 for a $FSK_{modulation}$ signal folowing the FSK signal of the Figure 3.15.

3.5.1 VCO setting

VCO of the PLL must provides at its output a square signal whose frequency varies between f_{min} = 1900 Hz and f_{max} = 2300 Hz in order to be sure to cover *mark* and *space* frequencies. See data sheet to understand the operation of the CD4046 and to determine R_1, R_2 and C_1 to obtained a VCO frequency which can go from 1900 Hz to 2300 Hz ($f_{max} - f_{min} = 2\Delta f_L = 400Hz$). The circuit of the CD4046 used as a VCO is given in figure 3.17.

Use the data sheet of the CD4046 to choose R_1, R_2 and C_1 :

1. Knowing f_{max} and f_{min}, what is the ratio $\frac{R_2}{R_1}$? Give the value of R_1 for $R_2 = 10k\Omega$.
2. Knowing Vdd = 10V (+5V - - 5V), f_{min} =1900 Hz and $R_2 = 10k\Omega$, give the C_1 value.
3. How can we adjust the central frequency ?
4. What happens if we decrease R_1 ?

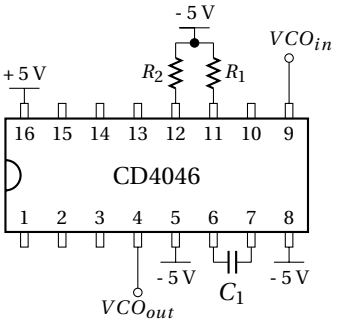


Figure 3.17: CD4046 used as a VCO.

3.5.2 Loop filter and PLL response

We will first use the XOR phase comparator (type I) of the CD4046 associated to a one pole filter (Fig. 3.18).

*Capture range : frequency range where the PLL is able to lock-in, starting from unlocked condition.
†ζ is the damping factor of the locked PLL response.

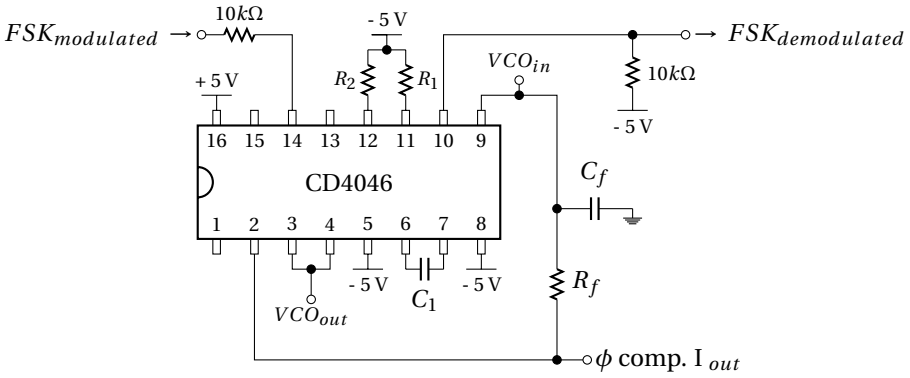


Figure 3.18: PLL locked using the type I comparator associated to a 1^{st} order filter.

1. Give the value of the product of phase detector gain K_p [V/Rad] and the VCO gain K_v [Rad/V.s] : $K = K_p \times K_v$.
2. Give the value of R_f for a 100 nF C_f capacitor of the loop filter knowing that $Q = 0.5$.
3. Give the theoretical value of the frequency lock range $2\Delta f_L$ *
4. Where must be the *mark* and *space* frequencies relatively to the locked range ?
5. What is the natural frequency f_n of the loop in the case of a one pole RC filter ?

3.6 PLL as a frequency multiplier

To recover a clock signal from transmitted digital data, it could be interesting to use a PLL as a frequency multiplier. The scheme of a frequency multiplier is given in figure 3.19.

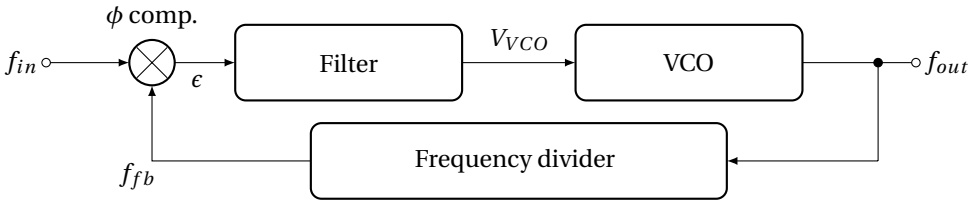


Figure 3.19: Frequency multiplier.

3.6.1 PLL with one pole - one zero loop filter

We start with the circuit of a simple PLL with a **type I phase comparator and a one pole filter**.

1. Give the value of R for a capacitor $C_1 = 2nF$ to have a $f_0 = 20$ kHz.

Express the loop gain of the PLL with one pole filter as in figure 3.20 with $R_f = 15k\Omega$ and $C_f = 100nF$.

2. Compute the value of $K = K_v K_p$.
3. What is the quality factor of the loop?
4. What is the natural frequency of the loop?
5. Compute the lock ranges.

We replace the one pole filter $R_f C_f$ by a **one pole one zero filter** (Fig. 3.21)

*Lock range : frequency range where the PLL is able to stay locked.

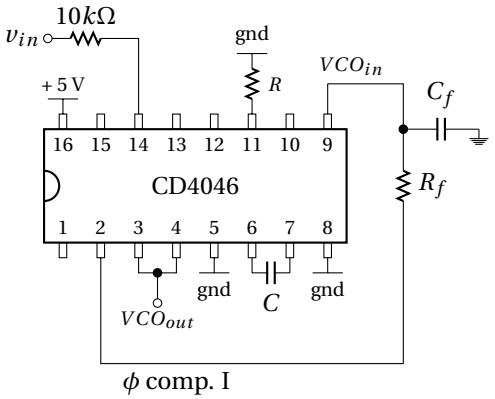


Figure 3.20: PLL locked using the type I comparator associated to a 1^{st} order R_f and C_f filter.

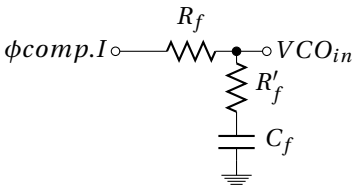


Figure 3.21: Filter 1 pole 1 zero.

6. Compute the loop gain with a type I comparator and a one pole one zero filter.

7. How to choose R'_f (R_f and C_f stay the same as for one pole filter) to have $Q = 0.5$?

3.6.2 Loop with multiplication

Now we want to synthesize a frequency of 20 kHz from a reference frequency F_{ref} submultiple of F_{out}. The circuit of the multiplier (by N) is given on figure 3.22. A divider by N is placed between the output of the VCO (pin 4) and the input of the phase comparator (pin 3) as in the figure 3.19. By doing this, we force the VCO to provide a frequency N times larger than the reference one (Eq. 3.23).

The loop with the type I comparator has the disadvantage to ring on harmonics of the input signal. To avoid this problem, it is preferable to use a loop with a type II phase comparator.

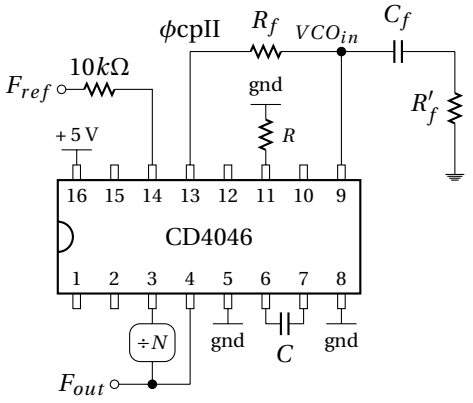


Figure 3.22: PLL as a frequency multiplier.

$$F_{out} = F_{VCO} = N.F_{ref} \tag{3.23}$$

Considering N values : 1, 2, 4, 6, 8 and 10. A CMOS divide by N counter CD4018 will be used.

1. Compare the expression of the transfer function of the PLL multiplier given in figure 3.22 with those without divider.
2. What is the value of the damping factor if we keep the previous R_f, R'_f, C values of the loop filter?
3. Give the value of the lock range for each cases :
   - $N = 1$ and $F_{ref} = 20kHz$
   - $N = 2$ and $F_{ref} = 10kHz$
   - $N = 4$ and $F_{ref} = 5kHz$
   - $N = 6$ and $F_{ref} = 3.3kHz$
   - $N = 8$ and $F_{ref} = 2.5kHz$
   - $N = 10$ and $F_{ref} = 2kHz$
4. See the data sheet of the CD4018 and suggest a diagram using this device to perform the division by N.

3.6.3 Frequency synthesizes

To synthesize a frequency, which is not necessarily a submultiple frequency of a reference frequency F_{ref}, a second frequency divider (by M) is required. Then, the synthesize frequency could be express as equation 3.24.

$$F_{out} = \frac{N}{M} \times F_{ref} \tag{3.24}$$

The multiplication by N has been previously studied. To build the divider by M, an other CD4018 could be used, at the input of the PLL ($\frac{F_{ref}}{M}$) or after the PLL ($\frac{NF_{ref}}{M}$). Consider a goal synthesis frequency of $\frac{5F_{ref}}{3}$.

- Which of the two solutions is the preferred one to be used for $F_{ref} = 1kHz$, $10kHz$ and $30kHz$?

Lab work

3.7 Frequency Shift Keying (FSK) demodulation

3.7.1 FSK demodulation using a CD4046 PLL

Now, we will study the FSK demodulation by using a CD4046 PLL integrated circuit.

VCO of the CD4046 supply a signal frequency from $1900Hz$ to $2300Hz$ which includes f_{mark} and f_{space}.

- $f_{min} = 1900Hz$
- $f_{max} = 2300Hz$

VCO setting

1. Start to build the VCO as in figure 3.23 with $C_1 = 90nF$ and $R_2 = 10k\Omega$ and $R_1 = 27k\Omega$. To do the VCO setting, apply successively $-5V$ and $+5V$ to the VCO input and measure the output with the frequency meter. Adjust the R and C values to cover f_{min} and f_{max} range.

2. Measure the VCO frequency for -5V, -2.5V, 0V, 2.5V and 5V input VCO_{in}.

3. Use a ramp signal going from -5V to +5V to see the evolution of the frequency in VCO_{out}.

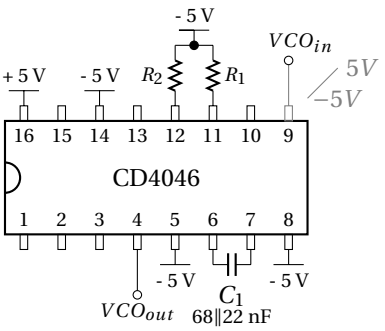


Figure 3.23: VCO part of the CD4046

3.7.2 Frequency Shift Keying (FSK) signal using the function generator

Use the "CH1" of the function generator as a square signal $\pm 5V$ (VCO_{in} centered in 0V) at 2 kHz.
Switch to the modulation function "MOD" (type "FSK") :

- "Fsk Rate" = 150 Hz (use 0.1 Hz to measure f_{mark} and f_{space} with multimeter.)
- "Hop Freq" = 2.2 kHz

So, FSK modulation is emulated by the function generator.

- Check the good operation of the modulation by seting the "Fsk Rate" at $0.1Hz$. During the 5s of each half period, f_{mark} and f_{space} are measured using the frequency meter.

After f_{mark} and f_{space} setting, increase the "Fsk Rate" to $150Hz$ to simulate a digital rate information of $300bit/s$.

☞ *A function generator is used here to emulate a frequency modulation. Note that a VCO can also do the job !*

PLL with type I comparator

Figure 3.24 shows the PLL connected with a type I comparator and a one pole loop filter. $R_f = 3.3k\Omega$ and $C_f = 100nF$. From the previous figure (3.23) remove the $-5V$ of the $pin14$ and add a $10k\Omega$ resistor to applied the FSK signal to the comparator, and thus to the PLL.

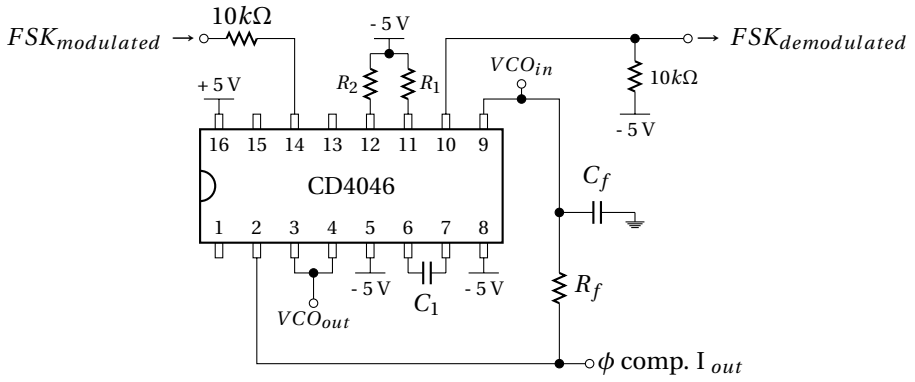


Figure 3.24: PLL locked using the type I comparator associated to a 1^{st} order filter.

2. Measure the lock range ($2\Delta f_L$) and the capture range ($2\Delta f_C$) of the loop. To do this, apply a $\pm 5V$ square signal instead of the FSK modulated signal. Varying the frequency of this signal and check the two input of the comparator simultaneously. Check that f_{mark} and f_{space} are in the capture range.
3. Measure the frequency for which the PLL is unlocked.
4. Mesure the shape of the output of the comparator in correspondence with the input signal and the VCO output for frequency going from f_{min} to f_{max}.
5. Connect the FSK modulation to the input of the PLL. Measure the overshoots on the $FSK_{demodulation}$ for a low frequency bit rate. Deduce if the damping factor of the loop is large or small as compared to 1.
6. Increase progressively the bit rate up to 300 bit/s (150 Hz). See the output signal. Conclude.
7. What is the maximum bit rate achievable?

8. We want to increase the band-width of the loop. To do this, we reduce the resistance R_f to achieve effectively a 300 bit/s. What happen ?

☞ Disassemble

3.8 Frequency multiplier

3.8.1 PLL with one pole - one zero loop filter

1. Start to build the VCO as given on figure 3.25. Adjust the R value to obtaine a $f_0 = 20kHz$ with a $C = 2.2nF$ (the input of the VCO is fixed to 2.5 V). R is composed of a $4.7k\Omega$ resistor in series with a $10k\Omega$ potentiometer.

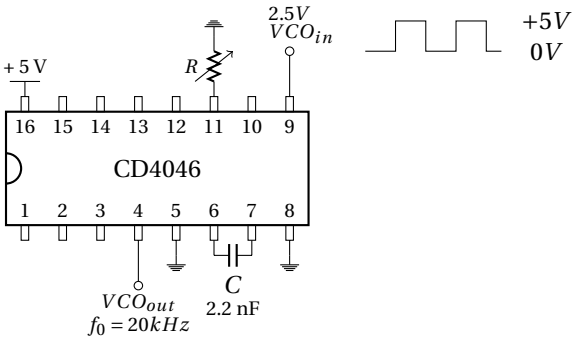


Figure 3.25: VCO.

Then build the PLL as given on figure 3.26 :

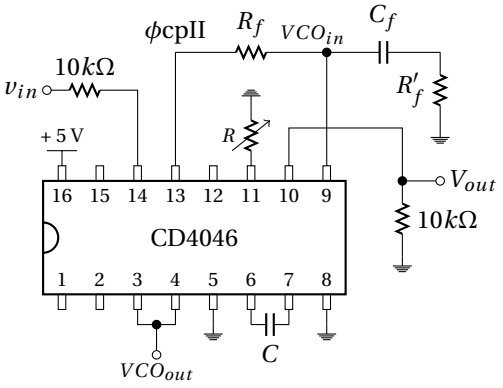


Figure 3.26: PLL locked using the type II comparator associated to a one pole one zero R_f, R'_f and C_f filter.

2. Close the loop with the R_f, R'_f and C_f one pole one zero filter. $R_f = 5.6k\Omega$, $R'_f = 1.6k\Omega$ and $C_f = 100nF$. Applied to the PLL input a $0-5V$ square signal. Measure the capture range by sweeping the square frequency. Observe the two phase detector inputs. See also the output of the V_{out} signal when the loop unlocks. Comment.

3.8.2 Loop with multiplication

Now we want to synthesize a frequency of 20 kHz from a reference frequency F_{ref} submultiple of F_{out}. The circuit of the multiplier (by N) is given on figure 3.27 with $R_f = 27k\Omega$, $R'_f = 4.7k\Omega$ and $C_f = 1\mu F$.

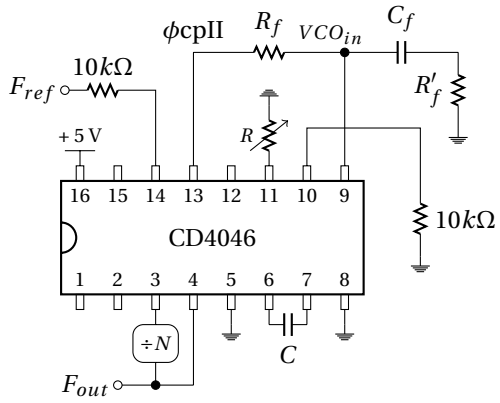


Figure 3.27: PLL as a frequency multiplier.

Divider by N is realized by a CD4018 as shown on figure 3.28.

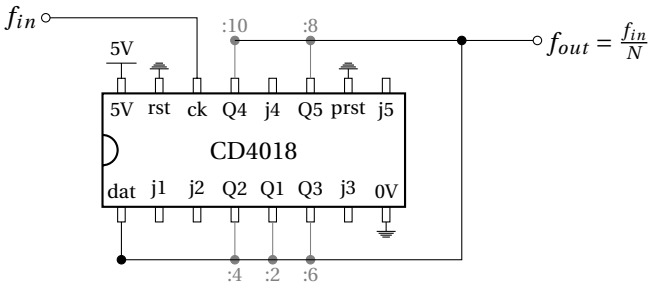


Figure 3.28: CD4018 as a divider by 1, 2, 4, 6, 8 and 10. "dat" need to be connected to the alone Qx corresponding to the desired N value.

Give the value of the lock and capture range for each cases :

1. $N = 1$ and $F_{ref} = 20kHz$
2. $N = 2$ and $F_{ref} = 10kHz$
3. $N = 4$ and $F_{ref} = 5kHz$
4. $N = 6$ and $F_{ref} = 3.3kHz$
5. $N = 8$ and $F_{ref} = 2.5kHz$
6. $N = 10$ and $F_{ref} = 2kHz$

3.8.3 Frequency synthesizes

To synthesize a frequency, which is not necessarily a submultiple frequency of a reference frequency F_{ref}, a second frequency divider (by M) is required. then, the synthesize frequency could be expressed as equation 3.25.

$$F_{out} = \frac{N}{M} \times F_{ref} \tag{3.25}$$

The multiplication by N is realized by the previous circuit. To do the divider by M, an other CD4018 is used between F_{ref} and the input of the PLL ($\frac{F_{ref}}{M}$).

- Considering a goal synthesis frequency of $\frac{5F_{ref}}{3}$, fixe N=10 and M=6.

☞ Disassemble and clean

Part IV

Modulation

4 Modulation

4.1 Introduction

MODULATION is a technique used in **electronic communications** for **transmitting informations** by using a **higher frequency carrier** such as a radio wave. This frequency transposition (Fig. 4.1) of the information signal (baseband signal) to a higher frequency band (radio frequency) allows to transmit it, through an **electromagnetic medium**. So, the carrier can be physically transmitted.

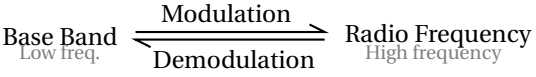


Figure 4.1: Modulation as a transposition frequency from baseband to radio frequency.

For communication between satellites and ground station, a carrier higher than some 10 MHz is required due to ionospheric opacity (figure 4.2). In radio communications or switched telephone network for instance, electrical signals can only be transferred over a limited pass-band frequency spectrum, with specific lower and upper cutoff frequencies (channel).

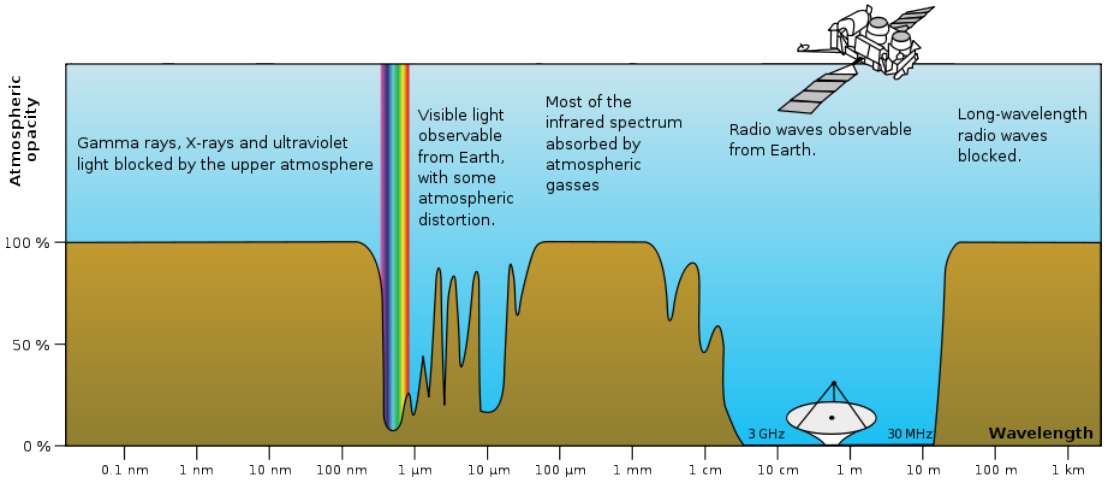


Figure 4.2: Radio atmospheric windows - `from wikipedia`

Modulation could have other application than electromagnetic transmission, for example for **fre-**

quency division multiplexing[*]. There is also somme cases where the modulation is used to down convert (at lower frequency) a use-full high frequency signal. This **down conversion** facilitates data-processing as **sampling, filtering, detection** (*lock-in amplifier*[†]) or **amplification** (*parametric amplifier*[‡] ; **mixer**[§]).

Many parameters can be modulated. In the case of simple sine wave (or square wave) carrier, there are three obvious parameters than can be varied :

- **Frequency** modulation (or Frequency-Shift Keying) - the frequency of the carrier signal is varied in accordance to the instantaneous amplitude of the modulating signal. A VCO could be used to do a frequency modulation and a PLL to do the demodulation as we have seen in the last practical work for the FSK demodulation.
- **Phase** modulation (or Phase-Shift Keying) - the phase shift of the carrier signal is varied in accordance to the instantaneous amplitude of the modulating signal.
- **Amplitude** modulation (or Amplitude-Shift Keying for digital modulation) - the amplitude of the carrier signal is varied in accordance to the instantaneous amplitude of the modulating signal.
  - Double-SideBand (DSB)
    - DSB modulation with carrier - used for the AM radio broadcasting band
    - DSB modulation with Suppressed-Carrier (DSB-SC) - to reduce the transmitted power
  - Single-SideBand (SSB)
    - SSB modulation with carrier - one sideband suppressed to reduce occupied channel bandwidth
    - SSB modulation with Suppressed-Carrier (SSB-SC) - to reduce both power and bandwidth

4.2 Amplitude modulation

A continuous wave radio-frequency signal (a sinusoidal carrier wave) has its amplitude modulated by the input waveform before transmission. Input waveform changes the amplitude of the carrier wave and creates the envelope of the waveform. A simple form of amplitude modulation, often used for digital communications, is *on-off keying*[¶]. For instance, this is used by radio amateurs to transmit Morse code.

Without transmission of the carrier, this modulation is obtained by simple **multiplication of an input signal by carrier signal**. Figure 4.3 shows waveform and spectrum of a multiplication of a sine-wave input signal (f_s) by a sine-wave carrier (f_0).

Indeed, multiplication transposes the input signal S at each side of the C carrier frequency (frequency domain). Each sideband is equal in bandwidth, and is a mirror image of the other. Moreover, for demodulation consideration, the carrier is generally added (see figure 4.4 and equation 4.1 with $1/k$ a factor corresponding to the proportion of carrier added) forming a full amplitude modulation AM, with carrier transmission, as waveform illustrated at the end of the figure 4.3.

$$AM \equiv S \times C + \frac{C}{k} \qquad \text{(DSB with carrier)} \tag{4.1}$$

Most of the time, the carrier signal C is only a sine wave as expressed in equation 4.2.

$$C = C_0 \sin\left(2\pi f_0 t\right) \tag{4.2}$$

[*]Frequency division multiplexing is a technique by which the total bandwidth available in a communication medium is divided into a series of non-overlapping frequency sub-bands (channels), each of which is used to carry a separate signal.

[†]A lock-in amplifier is a type of amplifier that can extract a signal with a known carrier wave from an extremely noisy environment. It uses mixing, through a frequency mixer, to transpose the input signal to low-frequency.

[‡]Parametric amplifier is a highly sensitive ultra-high-frequency or microwave amplifier having as its basic element a device whose reactance can be varied periodically following a pumping frequency.

[§]A frequency mixer is a nonlinear electrical circuit that creates new frequency signals at the sum and difference of the original frequencies (as a multiplier).

[¶]A type of amplitude-shift keying in which binary data is represented by the presence or absence of a carrier.

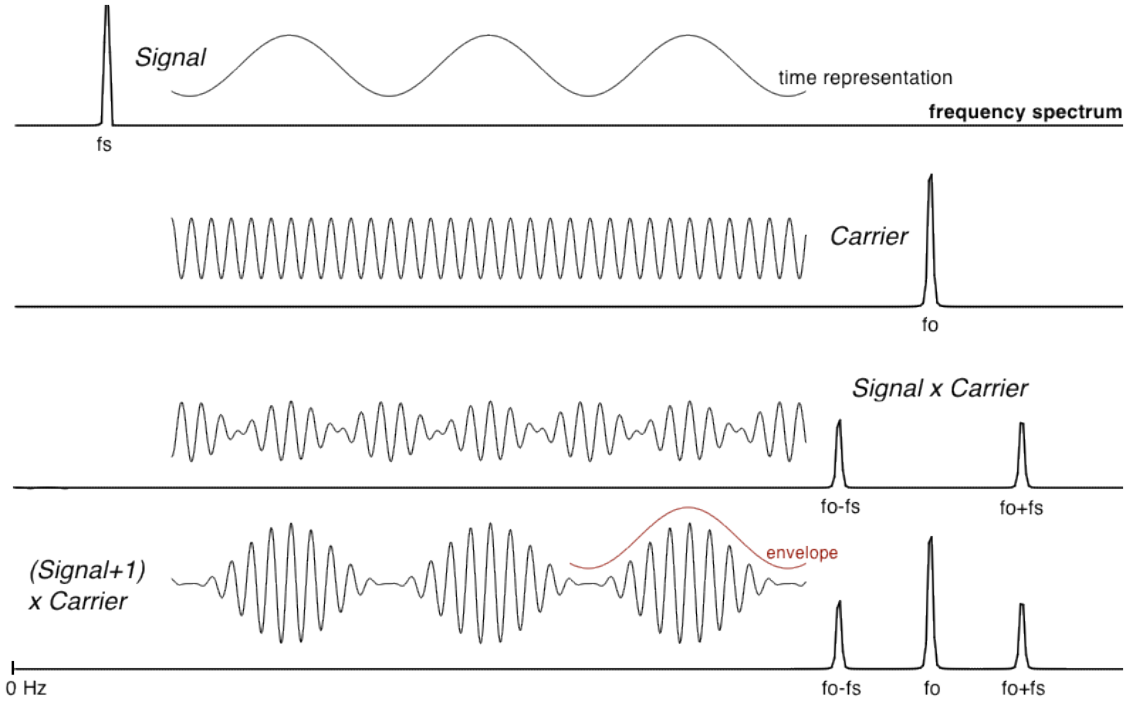


Figure 4.3: Time waveform and spectrum of a double side band (DSB) amplitude modulation without ($S \times C$; $k = \infty$) and with ($S \times C + C$; $k = 1$) transmission of the carrier.

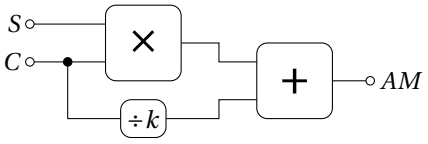


Figure 4.4: Scheme of amplitude modulator.

Input signal could also be expressed (Eq. 4.3) as a single tone signal for a simple example (Figures 4.3 and 4.5).

$$S = S_0 \sin\left(2\pi f_S t\right) \tag{4.3}$$

In these conditions, amplitude modulation is given by equation 4.4.

$$\begin{aligned} AM &\equiv S_0 \sin\left(2\pi f_S t\right) \times C_0 \sin\left(2\pi f_0 t\right) + \frac{C_0}{k} \sin\left(2\pi f_0 t\right) \\ &\equiv \underbrace{\frac{S_0 C_0}{2}\left[\cos\left(2\pi(f_0 - f_S)t\right) - \cos\left(2\pi(f_0 + f_S)t\right)\right]}_{\text{SideBands}} + \underbrace{\frac{C_0}{k}\sin\left(2\pi f_0 t\right)}_{\text{Carrier}} \end{aligned} \tag{4.4}$$

Using trigonometric functions*, equation 4.4 clearly shows that amplitude modulation produces, in addition to the adjacent sidebands $f_0 - f_S$ and $f_0 + f_S$, a signal with power concentrated at the carrier frequency f_0. Amplitude modulation resulting in two sidebands and a carrier is called *double side band amplitude modulation* (DSB). This simplest kind of amplitude modulation is **inefficient** because of the large fraction of wasted power for transmission of the carrier and in the redundancy of information signal in the two sidebands.

*$\sin(a)\sin(b) = \frac{\cos(a-b)-\cos(a+b)}{2}$

Increasing the efficiency : The carrier and/or one sideband may be suppressed at the expense of increased transmitter and receiver complexity. For reception, suppression of the carrier imply to restore it by the use of a local oscillator generated by a phase locked loop for example. Whereas in the case of carrier transmission, a simple rectifier diode could be used for demodulation (detection).

Suppressing both the carrier and one of the sidebands also reduces bandwidth occupancy. This is single-sideband modulation (SSB), widely used in amateur radio and other low consumption communication applications. This could be obtained by using a IQ modulator*.

4.2.1 Modulation index

The modulation index (also called "modulation depth") quantify the evolution of the carrier signal around its unmodulated level. It is defined differently in frequency and amplitude modulation. In the case of amplitude modulation, modulation index m is the ratio between the **"envelope" amplitude** S_0C_0 and the **unmodulated transmitted carrier amplitude** $\frac{C_0}{k}$ (defined as expression 4.5).

$$m = \frac{S_0 C_0}{C_0/k} = kS_0 \tag{4.5}$$

Indeed, modulation index referred to a normalized comparison between modulation amplitude and carrier amplitude. So, the expression 4.4 could be rewrite by factoring C which is common to the envelope amplitude and to the carrier (eq. 4.6). Finally, a normalization of the carrier amplitude added, leads to highlight m :

$$AM \equiv C_0 \sin\left(2\pi f_0 t\right)\left[\frac{1}{k} + S_0 \sin\left(2\pi f_S t\right)\right] = \frac{C}{k}\left[1 + \underbrace{kS_0}_{\text{m}} \sin\left(2\pi f_S t\right)\right] \tag{4.6}$$

So if carrier amplitude varies by 50% above and below its "unmodulated level", the modulation index is equal to 0.5. $m = S_0$ in the case of full adding of the carrier *i.e.* $k = 1$. Figure 4.5 shows in time domain and frequency domain, the waveform of amplitude modulation for different modulation index.

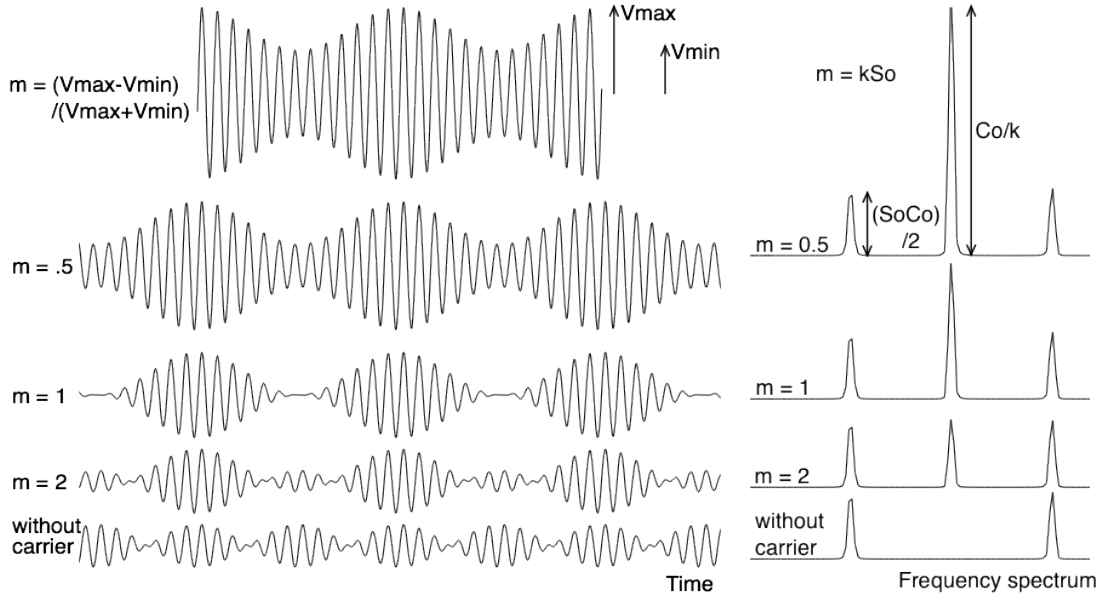


Figure 4.5: Different modulation index, from 50% (m = 0.5) to 200% (m = 2) and without carrier (m = ∞) in time domain and frequency domain. Amplitude of the unmodulated transmitted carrier amplitude C_0/k is clearly visible in the center frequency f_0. Amplitude of the side bands S_0C_0 are divided by two for each side band ; due to $\sin(a)\sin(b) = \frac{1}{2}(\cos(a-b) - \cos(a+b))$.

*A IQ modulator, for in-phase (I) and quadrature (Q), is a modulation using two carrier shifted in phase by $\pi/2$.

Given in the frequency domain (Fig 4.5), the amplitude at each frequency can be easily obtained by using the equation 4.4. Techniques to graphically estimate the modulation index are also reported on this figure for m ≤ 1 (usual case).

Graphic estimation of the modulation index given by expression 4.7 is easy to use for $m \leq 1$. However, if $m > 1$, it could be more complicated to estimate V_{max}, V_{min}, and therefore m. In practice, the modulation index is usually < 1 to avoid distortions and noise.

$$m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}} \quad \begin{cases} \text{with } S_0 C_0 = \frac{V_{max} - V_{min}}{2} \\ \text{and } \frac{C_0}{k} = \frac{V_{max} + V_{min}}{2} \end{cases} \tag{4.7}$$

Indeed, if the modulation index is larger than 100%, the input signal is distorted and could not be demodulated correctly. But a too small modulation index leads to a large fraction of the transmitted power put in the useless carrier signal alone. So, a good tradeoff could correspond to a modulation index between 1 and 0.1.

✏ *in the case of AM without carrier ($1/k = 0$), the modulation index is ∞.*

4.3 Amplitude demodulation

Demodulation is used to recover the information content (S) from the modulated carrier wave. Demodulation is traditionally used in connection with radio receivers, but many other systems need demodulators.

There are two main methods used to demodulate AM signals :

1. Envelope detection
2. Multiplication

4.3.1 Envelope demodulation

An amplitude modulated signal can be **rectified** without requiring a coherent* demodulator. For example, the signal can be passed through an envelope detector : a rectifier diode D (or a diodes bridge) and a low-pass RC filter as shown on figure 4.6. The output S' follows the same shape as the input baseband signal S (Fig. 4.7). Only a DC *offset* (inversely proportional to the modulation index) remains and is easily removed by using a high pass filter (as a coupling capacitor). Note that the polarity of the diode does not matter in the presented case of single-phase rectifiers.

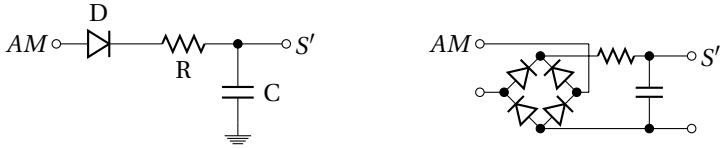


Figure 4.6: Scheme of a simple envelope demodulator. Single phase (left) and full-wave (right) rectifiers.

Rectifying can be modelized by an absolute value function† : absolute value || and a low pass filtering noted "LPF" in the equations. So, envelope detection can be expressed as equation 4.8.

$$LPF\left[\left|S \times C + \frac{C}{k}\right|\right] \propto S + cst \tag{4.8}$$

*Coherence describes all properties of the correlation between physical quantities. In the case of amplitude demodulation, it referred to the need of use a local oscillator C' locked (synchronized) to the carrier C. As opposed to envelope demodulation which doesn't need local oscillator at all.

†Absolute value correspond in fact to a full-wave rectification requiring larger number of diodes. However, the single-phase rectification shown in figure 4.6 introduce a factor of 0.5 in the demodulated amplitude.

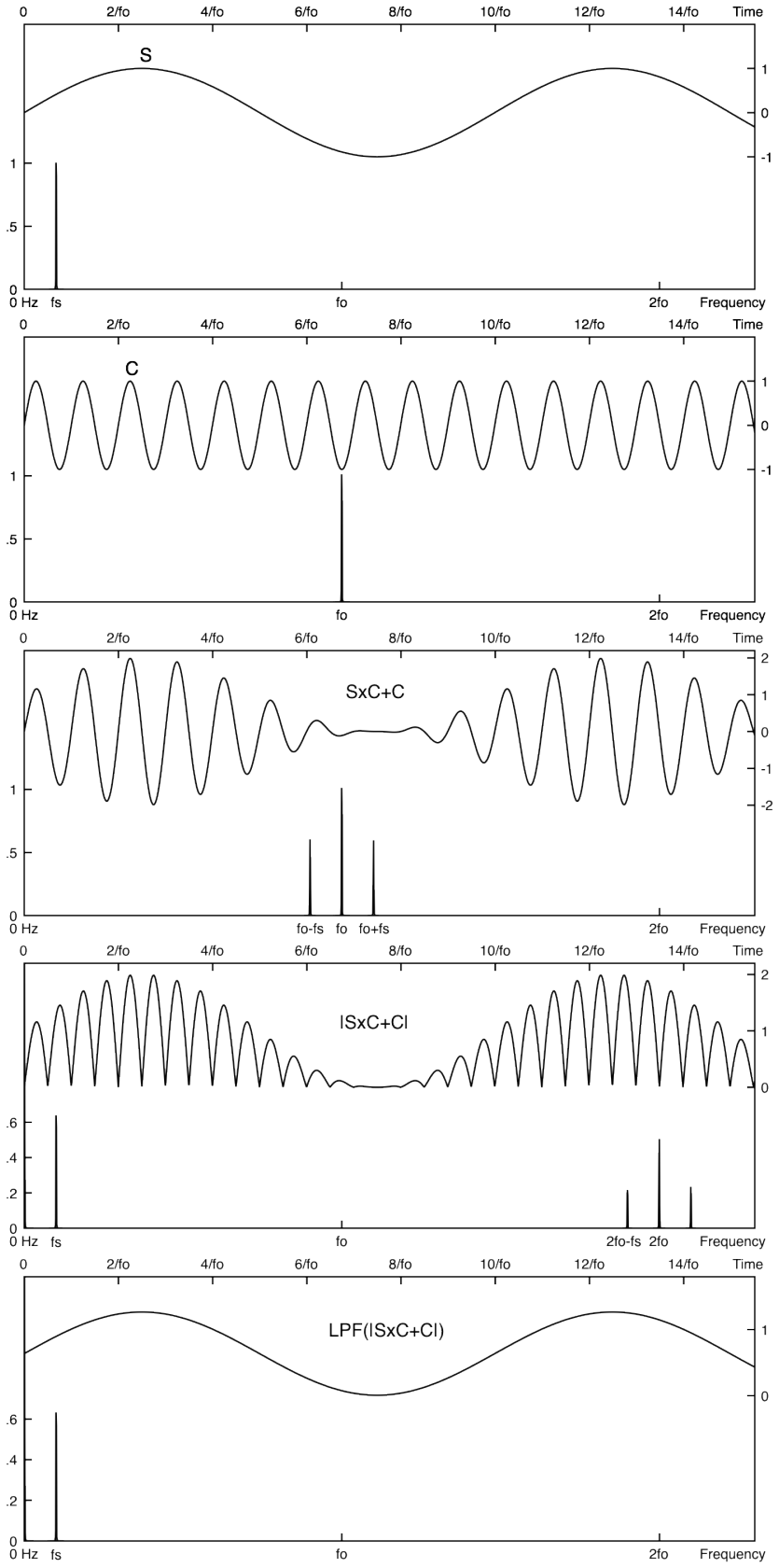


Figure 4.7: **Waveform of an envelope detection :** Signal S, Carrier C, AM with a unity modulation index S×C+C, Rectifying as an absolute value |S×C+C| and low pass filtering LPF(|S×C+C|) for a complete reconstruction of the input signal S.

- **The rectifier** may be in the form of a single diode D, or anything that will pass current in one direction only*.
- **The filter** is usually a RC low-pass filter when the difference in frequency between the signal and the carrier is very large†. Furthermore, the filter function can sometimes be achieved by the limited frequency response of the rectifier itself or of other part of the readout.

However, **only amplitude modulation with a modulation index smaller than 100% can be demodulated by envelope detection**. Indeed, for a modulation index larger than 100%, or downright without carrier, envelope detection introduces necessarily large distortions. Figure 4.8 shows, for example, a rectifying detection of an amplitude modulation without carrier (S×C). In this extreme case where $m = \infty$, the demodulated signal is roughly a sine wave, but at twice (!) the frequency of the input signal.

☞ To avoid this kind of distortions, a coherent demodulation is required.

4.3.2 Product demodulation

The product detector, illustrated by figure 4.9, **multiplies** the incoming modulated signal AM by the signal of a local oscillator C'. C' need to have the **same frequency as the carrier** C of the incoming signal.The original S signal is finally recover after low pass **filtering** (LPF) and suppression of the DC *offset* (eq. 4.9).

$$LPF\left[\left(S\times C+\frac{C}{k}\right)\times C'\right]\propto S+cst \tag{4.9}$$

Using the same example as for modulation equation 4.4 and for $C' = C$, a product detection before the filtering could be expressed as equation 4.10. Using trigonometric functions‡, this expression shows that the information content S is restored in the base-band f_S, while the carrier and harmonics are pushed around $2f_0$ and are therefore easily filtered.

$$\begin{aligned}
&C\times\left(S\times C+\frac{C}{k}\right)\\
&=C_0\sin\left(2\pi f_0 t\right)\left\{\frac{S_0C_0}{2}\left[\cos\left(2\pi(f_0-f_S)t\right)-\cos\left(2\pi(f_0+f_S)t\right)\right]+\frac{C_0}{k}\sin\left(2\pi f_0 t\right)\right\}\\
&=\frac{S_0C_0^2}{2}\left[\sin\left(2\pi f_0 t\right)\cos\left(2\pi(f_0-f_S)t\right)-\sin\left(2\pi f_0 t\right)\cos\left(2\pi(f_0+f_S)t\right)\right]\\
&\quad+\frac{C_0^2}{k}\sin^2\left(2\pi f_0 t\right)\\
&=\frac{S_0C_0^2}{4}\left[\sin\left(2\pi(2f_0-f_S)t\right)+\sin\left(2\pi f_S t\right)-\sin\left(2\pi(2f_0+f_S)t\right)+\sin\left(2\pi f_S t\right)\right]\\
&\quad+\frac{C_0^2}{2k}\left[1-\cos\left(2\pi 2f_0 t\right)\right]\\
&=\\
&\boxed{\frac{S_0C_0^2}{4}\Big[2\underbrace{\sin\left(\mathbf{2\pi f_S t}\right)}_{\text{baseband}}+\underbrace{\sin\left(2\pi(2f_0-f_S)t\right)-\sin\left(2\pi(2f_0+f_S)t\right)\Big]+\frac{C_0^2}{2k}\left[1-\cos\left(2\pi 2f_0 t\right)\right]}_{\text{radio frequency + DC}\rightarrow\text{filtered}}}
\end{aligned} \tag{4.10}$$

Figure 4.10 gives the waveform to illustrate this product detection in the particular case where $k = C_0 = S_0 = 1$. In this case, equation 4.10 can be simplified as equation 4.11. This last equation highlights the different spectral lines of the demodulated signal before filtering (DC, f_S, $2f_0 - f_S$, $2f_0$ and $2f_0 + f_S$).

*Many natural substances exhibit rectifiyng behavior, which is why envelope demodulation was the earliest demodulation technique used in radio.

†In the case of AM radio broadcast, a carrier from few 100 kHz to few MHz is used for 10 kHz signal bandwidth (audio.). Regarding satellite communications, frequency carrier is of the order of several GHz; far away the signal bandwidth. For these kind of applications of the modulation, a simple first order low-pass filter is generally enough to attenuate residuals carrier harmonics.

‡$\sin(a)\cos(b) = \frac{\sin(a+b)+\sin(a-b)}{2}$; $\sin^2(a) = \frac{1-\cos(2a)}{2}$; $\sin(-a) = -\sin(a)$

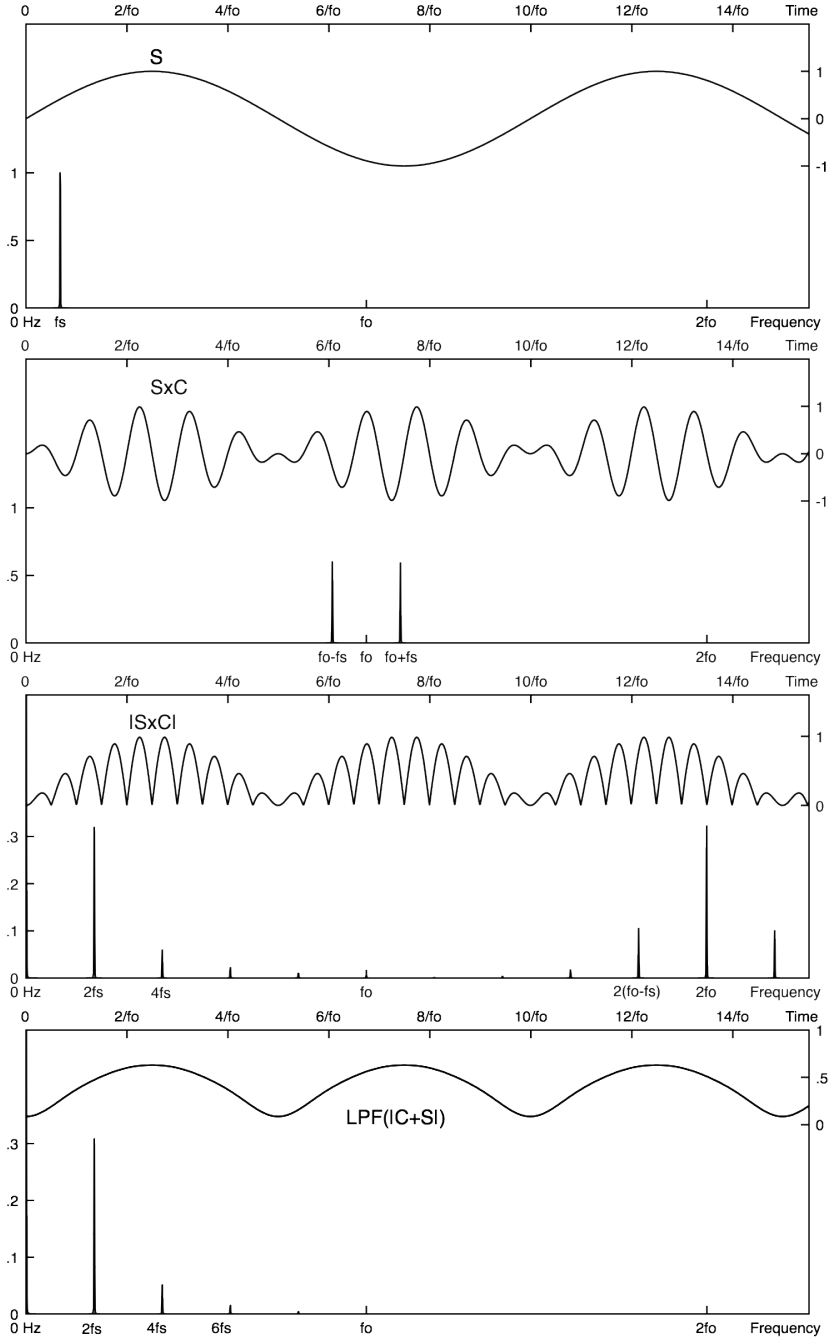


Figure 4.8: **Waveform of an envelope detection of an amplitude modulation without transmission of the carrier :** Signal S, AM without carrier S×C, Rectifying as an absolute value |S×C| and low pass filtering LPF(|S×C|). This figure clearly shows distortions introduced by envelope detection in the case of modulation index larger than 100%. Signal resulting from envelope detection is at twice the frequency of the input signal. We also can see other harmonics $4f_S$, $6f_S$, ... in the spectrum.

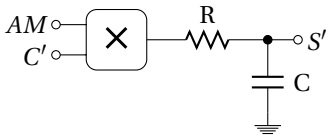


Figure 4.9: Simplified scheme of a product demodulator.

$$C \times (S \times C + C) \quad \text{with } C_0 \text{ and } S_0 = 1$$

$$= \underbrace{\frac{1}{2}}_{DC} + \underbrace{\frac{1}{2}\sin\left(2\pi f_S t\right)}_{f_S} + \underbrace{\frac{1}{4}\sin\left(2\pi(2f_0 - f_S)t\right)}_{2f_0 - f_S} - \underbrace{\frac{1}{2}\cos\left(2\pi 2 f_0 t\right)}_{2f_0} - \underbrace{\frac{1}{4}\sin\left(2\pi(2f_0 + f_S)t\right)}_{2f_0 + f_S} \tag{4.11}$$

The difference between envelope and product detection results on the **lower number of harmonics introduced by coherent technique as compared to rectifier**. Spectrum frequencies higher than $2f_0$ are shown in figure 4.11 for the two demodulation techniques. This comparison of the demodulated signal before filtering highlights harmonics at $4f_0$ introduced by rectifying.

But high frequency part of the spectrum can be easily filtered. Then the main difference between envelope and product detection is that the second technique can demodulate both amplitude modulation with or with-out carrier. So modulation without or with reduced carrier, *i.e.* with m > 100%, requires necessarily (to avoid distortion as shown on figure 4.8) this kind of coherent demodulation. Figure 4.12 shows demodulation of a modulated signal without carrier $(S \times C)$.

This product detection of a modulated signal without carrier can be expressed as equation 4.12. We see in this expression, the baseband demodulated signal and the radio frequency signal that we need to filter. Finally, it appears that there is no DC on this demodulated signal. This is due to the absence of carrier.

$$C \times S \times C$$

$$= C_0 \sin\left(2\pi f_0 t\right) \frac{S_0 C_0}{2} \left[\cos\left(2\pi(f_0 - f_S)t\right) - \cos\left(2\pi(f_0 + f_S)t\right)\right]$$

$$= \frac{S_0 C_0^2}{2} \left[\sin\left(2\pi f_0 t\right)\cos\left(2\pi(f_0 - f_S)t\right) - \sin\left(2\pi f_0 t\right)\cos\left(2\pi(f_0 + f_S)t\right)\right] \tag{4.12}$$

$$= \frac{S_0 C_0^2}{4} \left[\sin\left(2\pi(2f_0 - f_S)t\right) + \sin\left(2\pi f_S t\right) - \sin\left(2\pi(2f_0 + f_S)t\right) + \sin\left(2\pi f_S t\right)\right]$$

$$=$$

$$\boxed{\frac{S_0 C_0^2}{4}\left[2\underbrace{\sin\left(\mathbf{2\pi f_S t}\right)}_{\text{baseband}} + \underbrace{\sin\left(2\pi(2f_0 - f_S)t\right) - \sin\left(2\pi(2f_0 + f_S)t\right)}_{\text{radio frequency - filtered}}\right]}$$

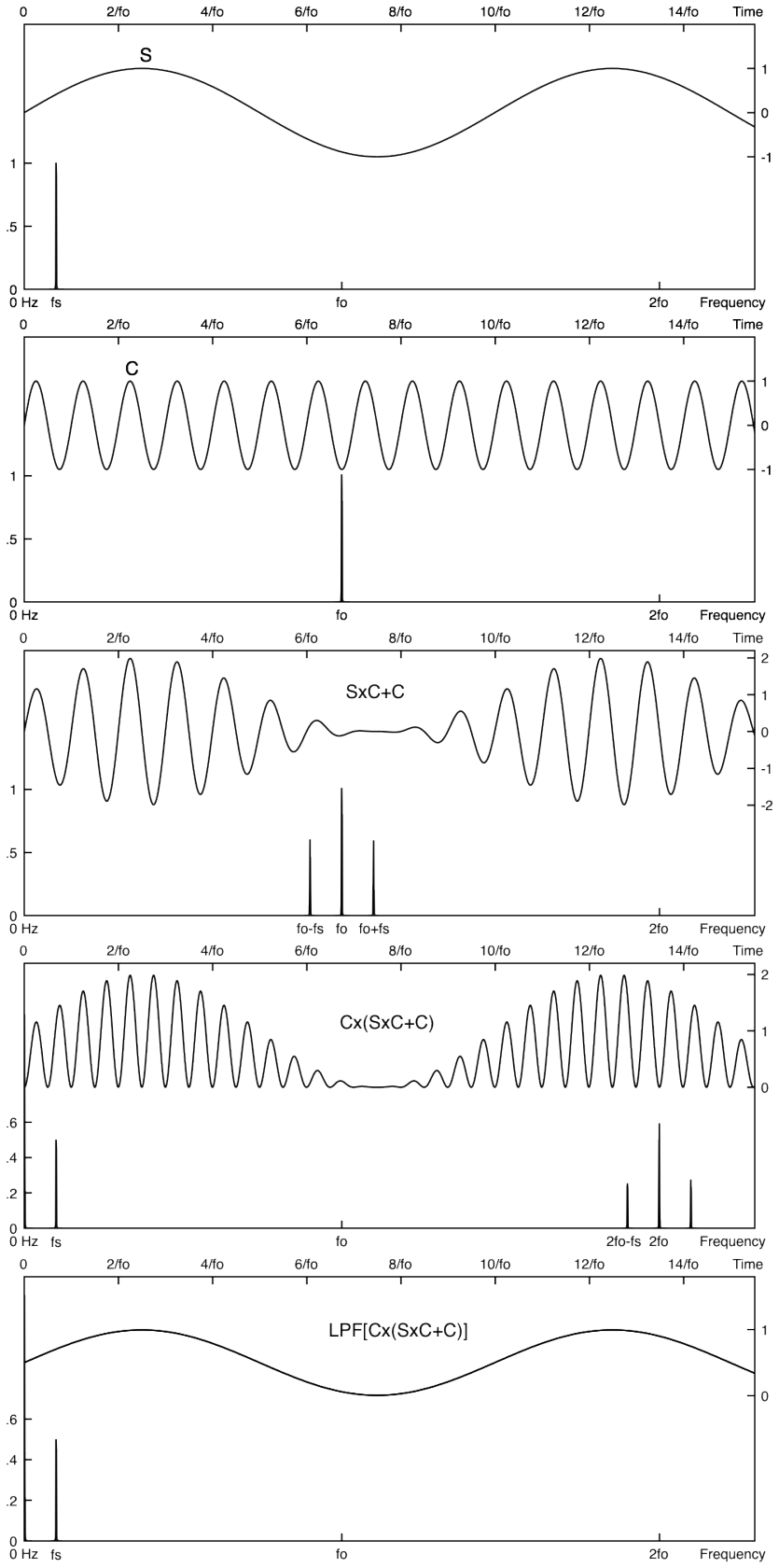


Figure 4.10: **Waveform of a product detection :** Signal S, Carrier C, AM signal S×C+C, demodulation C×(S×C+C) and low pass filtering LPF[C×(S×C+C)].

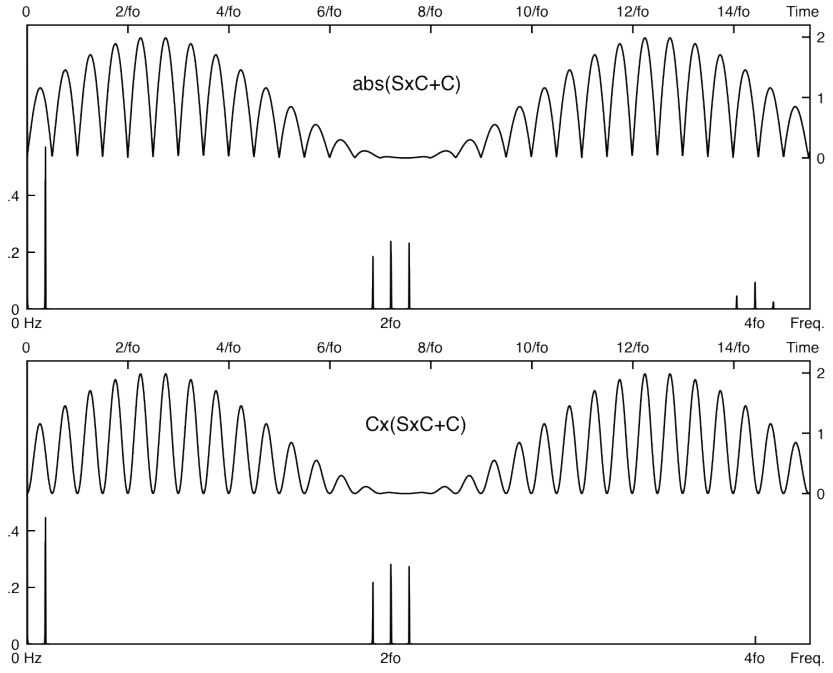


Figure 4.11: **Rectified** *vs* **Multiplied AM** demodulated signal. Rectifying introduce higher frequency harmonics. The difference is also visible on the lower part of the time frames.

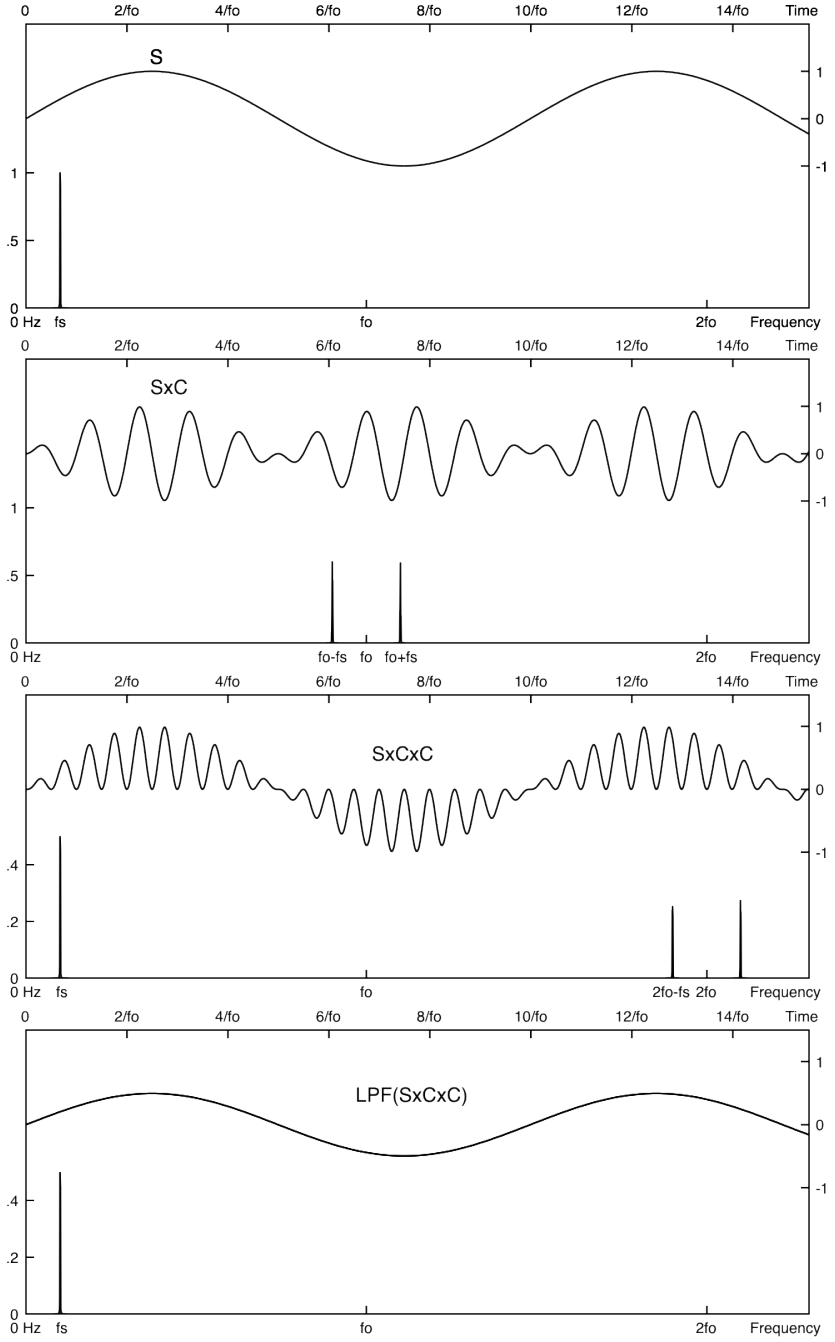


Figure 4.12: **Waveform of a product detection of an amplitude modulation without transmission of the carrier :** Signal S, AM without carrier S×C, Demodulation by product S×S×C and low pass filtering LPF(S×S×C). With this product detection, there is no distortion, even if the carrier is not transmitted. Moreover, due to the fact that there is no carrier, there is no DC signal (*offset*) associated to the demodulated signal S'.

Tutorial

We plan to transmit an information content (S) from $0-30kHz$ baseband frequencies to a radio channel (C) centered around $200kHz$.

4.4 Double Side Bande Amplitude Modulation

Considering S and C, two sine waves at $f_S = 30\ kHz$ and $f_0 = 200\ kHz$ respectively :

- $S = S_0 \cos\left(2\pi f_S t\right)$
- $C = C_0 \cos\left(2\pi f_0 t\right)$

4.4.1 Modulation without carrier transmission

Starting by a simple multiplication $AM_1 = S \times C$ as figure 4.13.

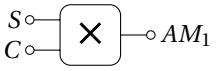


Figure 4.13: Modulation by simple multiplication.

1. Give the expression of $S \times C$ while revealing frequencies which form the modulated signal.
2. Plot the spectrum of AM_1.
3. What is the value of the modulation index ?
4. What happens if the carrier C is a square signal ? Plot the AM_1 spectrum in this case.
5. Now, plot the AM_1 spectrum in the case of a sin-wave carrier C, but with a non monochromatic input signal. Consider the spectrum of S given on figure 4.14.
6. What happens if the frequency carrier f_0 is lower than 30 kHz ? Plot the AM_1 spectrum in the case of a sine-wave carrier C at f_0 = 20 kHz. What can we expect from such a modulation ?

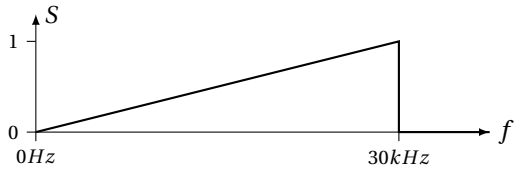


Figure 4.14: Spectrum of the information content S.

4.4.2 The use of an AD633 as multiplier

The AD633 device, is an analog multiplier including a summing input Z useful to add carrier for a complete amplitude modulation. The expression of the output pin W of the AD633 as a function of inputs is given on equation 4.13.

$$W = \frac{(X_1 - X_2) \times (Y_1 - Y_2)}{10V} + Z \tag{4.13}$$

Figure 4.15 gives the pin configuration of the AD633 and connections to build a simple multiplication $S \times C$. Inverting input X_2 and Y_2 are not used and connected to ground.

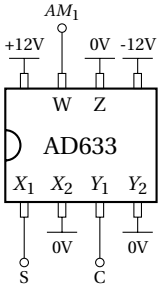


Figure 4.15: Pin configuration of an AD633 - Top view.

1. Considering $S = 6\text{V}\cos(2\pi\ 30\text{kHz}\ t)$ and $C = 10\text{V}\cos(2\pi\ 200\text{kHz}\ t)$; what is the numerical expression of the $AM_1(t)$ modulated signal ?
2. What would happen if S and C had an amplitude of $12V$?

4.4.3 Product detection

1. Propose a scheme using another AD633 to realize the demodulation of AM_1.
2. Plot the spectrum of the output of the second multiplier before filtering.
3. What is the cut-off frequency needed to restore S? Give numerical value of filter elements* needed to achieved a complete demodulation.
4. Plot the spectrum after filtering.

4.4.4 Modulation with carrier transmission using an AD633

A modulation with transmission of the carrier could be expressed as $AM_2 = \frac{C \times S}{10V} + C$.

1. Propose a simple modification of the scheme of the figure 4.15 to obtain AM_2, using a unique AD633 device.

*Choose R value = 1 $k\Omega$.

2. What is the numerical expression of the $AM_2(t)$ modulated signal showing the modulation index? What is the modulation index value ?

3. Plot the spectrum of AM_2.

4.4.5 Modulation index adjustment

Now, we want to change the modulation index of this amplitude modulation. To do that we used an operational amplifier (TL081) to adjust the amplitude of the carrier added to the product $S \times C$.

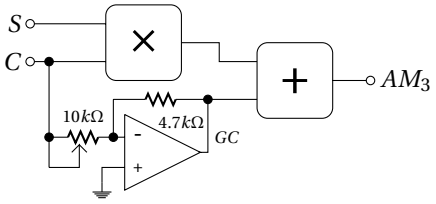


Figure 4.16: Scheme of amplitude modulator with adjustable modulation index.

1. Give the expression of the gain G obtained using the operational amplifier (10 $k\Omega$ potentiometer = R_1; 4.7 $k\Omega$ = R_2).

2. Give the expected range of modulation index m using the potentiometer from 0 Ω to 10$k\Omega$.

3. Taking into account the 50 Ω output impedance of the generator which supply C, what is the range of m ?

4. Using a TL081 as a variable gain amplifier; what is the cutoff frequency?

5. Plot the spectrum of AM_3 for an index modulation of 2, 1 and 0.5.

4.4.6 Enveloppe detection

Consider the rectifier of the figure 4.17 :

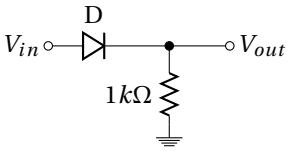


Figure 4.17: Scheme of a half wave rectifier.

1. Give the output voltage of the rectifier for a sine wave input signal (assuming that the diode is ideal - *i.e.* without threshold).

2. Give the output voltage in the case of a 0.6 V threshold voltage for a sine wave input signal of 0.5V, 1V and 6V amplitude.

3. What happens if we invert the polarity of the diode?

Now, we consider the envelope detector of the figure 4.18 with low pass filter:

4. Give the output voltage of the rectifier for a sine wave input signal (ideal diode).

5. What is the expression of the cutoff frequency f_c associated to the 10$k\Omega$ and C ?

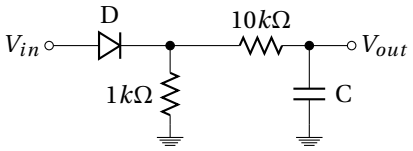


Figure 4.18: Envelope detector.

6. What happens for an input sine-wave of frequency smaller than f_c ?
7. Same question for an input sine-wave of frequency larger than f_c.
8. Plot the output signal (time domain) for a sine wave at a frequency = f_c.

We will use this detector to demodulate AM_3 with an index factor $m \leq 1$.

9. Considering $f_S = 30kHz$ and $f_0 = 200kHz$, what range of cutoff frequency do we need to demodulate AM_3 ?
10. Calculate C value for a first order $f_C = 50\ kHz$ low pass filter.
11. What is the attenuation of the first "carrier harmonic" ?

Lab work

4.5 Amplitude modulation as a simple multiplication

4.5.1 Modulation

Using the AD633 multiplier, achieve the multiplication 4.19 of two sine waves issued from the function generator :

CH_1 **:** sine wave of $200kHz$ and $10V_{pp}$

CH_2 **:** sine wave of $30kHz$ and $6V_{pp}$

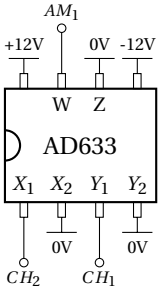


Figure 4.19: Pin configuration of an AD633 for multiplication (top view).

Check that the output of the AD633 correspond well to the multiplication of the two inputs. Use the FFT function of your oscilloscope (*Math function → FFT*) to watch the spectrum of this modulation.

1. Measure and plot the waveform and the spectrum of the obtained modulation.

2. Use a square signal on the CH_1 (carrier) instead of sine wave. Measure and plot the waveform and the spectrum of the modulation.

3. Restore the sine wave on CH_1, and change CH_2 (signal) from sine to square. Measure and plot the waveform and the spectrum of the modulation.

4. Finally, choose two square signals as for carrier and for signal. Comment.

4.5.2 Product detection

1. Build a second multiplier AD633 (as for modulation Fig. 4.19) to demodulate AM_1 (first part of the figure 4.20).
2. Measure and plot the waveform and the spectrum of the demodulated signal.
3. Build the R-C low-pass filter (Fig. 4.20) to attenuate carrier harmonics. Measure and plot the waveform and the spectrum of the filtered signal.
4. Same question using a square carrier.

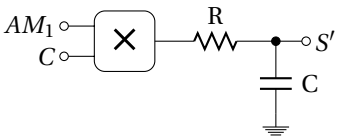


Figure 4.20: Product demodulator.

4.5.3 Modulation with adding carrier

A modulation with transmission of the carrier, and a unity modulation index, could be built using the scheme of the figure 4.21.

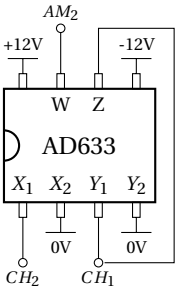


Figure 4.21: Pin configuration of an AD633 for amplitude modulation with carrier.

Build the modulator and check that the output of the AD633 correspond well to an amplitude modulation with carrier.

1. Measure and plot the waveform and the spectrum of the obtained modulation.

To adjust the index factor, a variable gain G between the signal from the CH_1 and the summing input Z is required. Build this variable gain amplifier, by using a TL081 biased under $\pm 12V$, following the scheme given in figure 4.22.

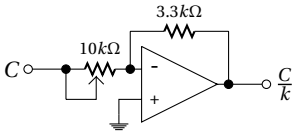


Figure 4.22: Scheme of variable gain amplifier.

Use this amplifier in the modulator between the CH_1 and the summing input Z. Observe the evolution of the index factor on the output of the modulator AM_3.

2. Plot the two extreme cases of index modulation reach.
3. Try to determine m_{min} and m_{max} by using time waveform. In practice, which effects limit the m range ?

4.5.4 Envelope detection

Build the rectifier folowing the figure 4.23 :

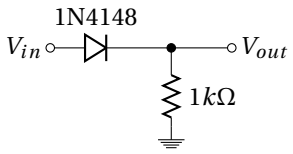


Figure 4.23: Scheme of a half wave rectifier.

1. Check the operation of the rectifier, using a $6V_{pp}$ sine-wave. Plot the waveform of the output signal V_{out}.
2. Place a capacitor in parallel with the resistor (Fig. 4.24) to obtain $f_C = 40kHz$. Measure this cutoff frequency.
3. Connect the modulated signal to the input of the rectifier. Measure and plot output waveform and spectrum of the rectifier with and without the capacitor. Repeat this measurement for a modulation index from 0.5, 1 to 2.
4. Increase the carrier frequency up to 2 MHz. what is happening ? comment.

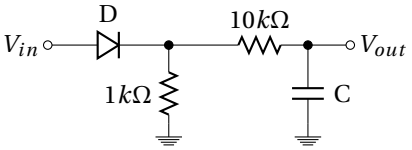


Figure 4.24: Envelope detector.

☞ Disassemble and clean

A

Polynomials filter tables

Butterworth, Chebyshev (3 dB and 1 dB), Bessel and Legendre polynomials tables needed for filter synthesis :

n	**Butterworth** polynomials
2	$s^2+1.4142s+1$
3	$(s+1)(s^2+s+1)$
4	$(s^2+0.7654s+1)(s^2+1.8478s+1)$
5	$(s+1)(s^2+0.618s+1)(s^2+1.618s+1)$
6	$(s^2+0.5176s+1)(s^2+1.4142s+1)(s^2+1.9319s+1)$
7	$(s+1)(s^2+0.445s+1)(s^2+1.247s+1)(s^2+1.8019s+1)$
8	$(s^2+0.3902s+1)(s^2+1.1111s+1)(s^2+1.6629s+1)(s^2+1.9616s+1)$
9	$(s+1)(s^2+0.3473s+1)(s^2+s+1)(s^2+1.5321s+1)(s^2+1.8794s+1)$

n	**Chebyshev** polynomials (ripple 3dB $\equiv \epsilon = 1 \rightarrow H_{0_{even\,\mathrm{n}}} = 2^{-0.5} \approx 0,707$)
2	$1.4125s^2+0.9109s+1$
3	$(3.3487s+1)(1.1916s^2+0.3559s+1)$
4	$(5.1026s^2+2.0984s+1)(1.1073s^2+0.1886s+1)$
5	$(5.6328s+1)(2.6525s^2+0.7619s+1)(1.0683s^2+0.1172s+1)$
6	$(11.2607s^2+3.2132s+1)(1.9164s^2+0.4003s+1)(1.0473s^2+0.0801s+1)$
7	$(7.9061s+1)(4.8959s^2+1.1159s+1)(1.5942s^2+0.2515s+1)(1.0347s^2+0.0582s+1)$
8	$(19.8831s^2+4.3139s+1)(3.1163s^2+0.5732s+1)(1.4213s^2+0.1747s+1)(1.0265s^2+0.0443s+1)$
9	$(10.1756s+1)(7.8967s^2+1.4585s+1)(2.365s^2+0.3561s+1)(1.3164s^2+0.1294s+1)(1.0209s^2+0.0348s+1)$

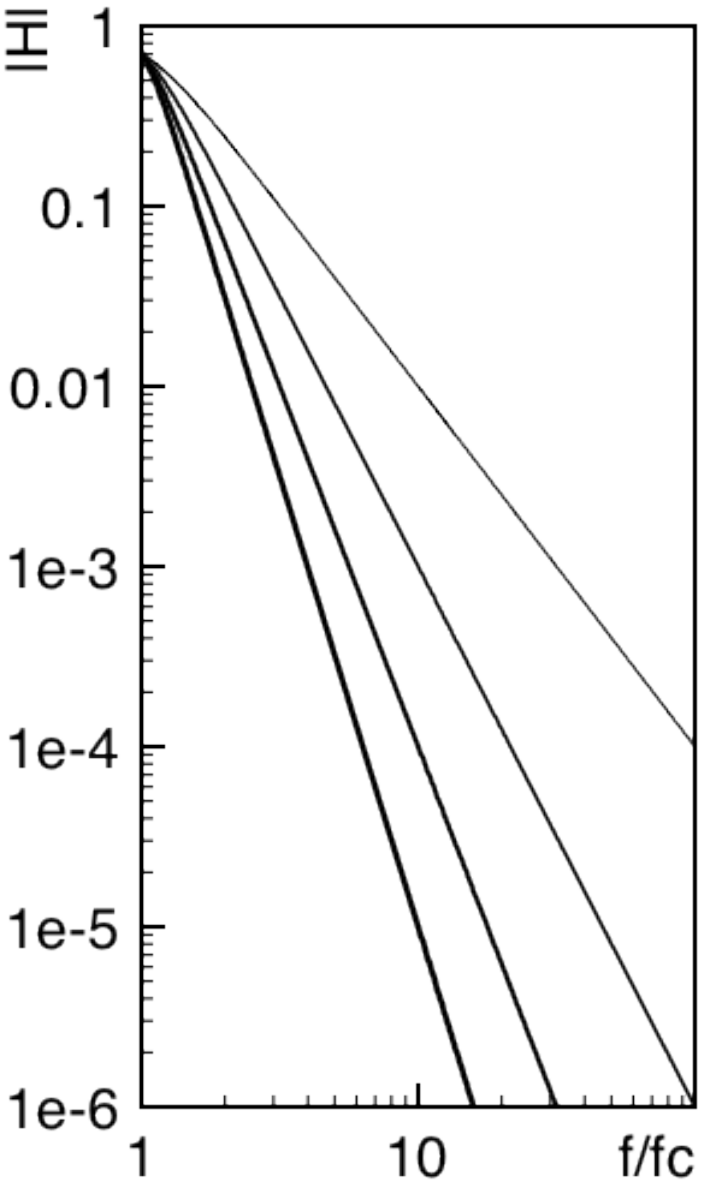
n	**Chebyshev** polynomials (ripple 1dB $\equiv \epsilon = 0.5 \rightarrow H_{0_{even\,\mathrm{n}}} = \frac{1}{\sqrt{1+0.5^2}} \approx 0,894$)
2	$0.907s^2 + 0.9956s + 1$
3	$(2.023s + 1)(1.0058s^2 + 0.497s + 1)$
4	$(3.5791s^2 + 2.4113s + 1)(1.0136s^2 + 0.2828s + 1)$
5	$(3.454s + 1)(1.0118s^2 + 0.181s + 1)(2.3293s^2 + 1.0911s + 1)$
6	$(1.793s^2 + 0.6092s + 1)(1.0093s^2 + 0.1255s + 1)(8.0188s^2 + 3.7217s + 1)$
7	$(4.868s+1)(1.0073s^2+0.092s+1)(1.5303s^2+0.3919s+1)(4.3393s^2+1.6061s+1)$
8	$(1.0058s^2 + 0.0704s + 1)(2.9337s^2 + 0.8754s + 1)(1.382s^2 + 0.2755s + 1)(14.2326s^2 + 5.0098s + 1)$
9	$(6.276s+1)(1.2896s^2+0.2054s+1)(1.0047s^2+0.0556s+1)(2.2801s^2+0.5566s+1)(7.0242s^2 + 2.1033s + 1)$

n	**Bessel** polynomials (normalised to 3dB attenuation at $\omega/\omega_c = 1 \rightarrow$ Cf lecture)
2	$0.618s^2 + 1.3616s + 1$
3	$(0.756s + 1)(0.4771s^2 + 0.9996s + 1)$
4	$(0.4889s^2 + 1.3396s + 1)(0.3889s^2 + 0.7742s + 1)$
5	$(0.665s + 1)(0.3245s^2 + 0.6215s + 1)(0.4128s^2 + 1.1401s + 1)$
6	$(0.2756s^2 + 0.513s + 1)(0.3504s^2 + 0.9686s + 1)(0.3887s^2 + 1.2217s + 1)$
7	$(0.593s+1)(0.238s^2+0.4332s+1)(0.301s^2+0.8303s+1)(0.3394s^2+1.0944s+1)$
8	$(0.2087s^2 + 0.3727s + 1)(0.2621s^2 + 0.7202s + 1)(0.2979s^2 + 0.9753s + 1)(0.3161s^2 + 1.1112s + 1)$
9	$(0.538s+1)(0.231s^2+0.6319s+1)(0.1854s^2+0.3257s+1)(0.2635s^2+0.8710s+1)(0.2834s^2 + 1.0243s + 1)$

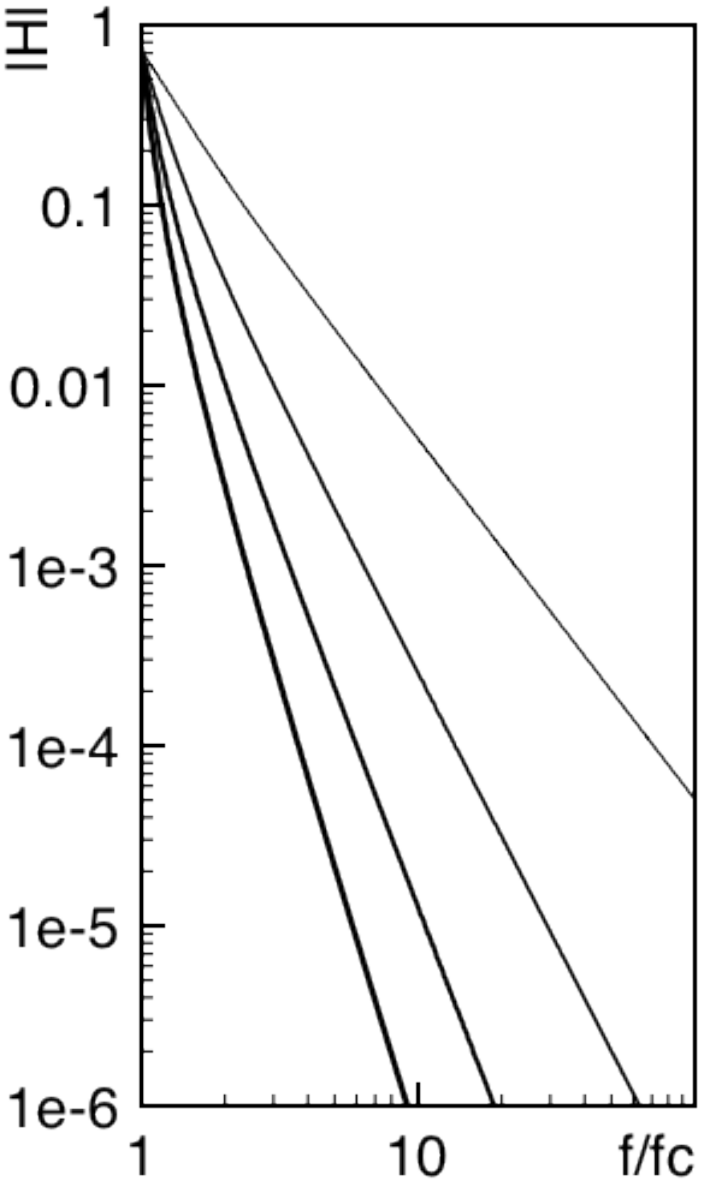
n	**Legendre** polynomials
2	$s^2 + 1.4142s + 1$
3	$(1.612s + 1)(1.0744s^2 + 0.7417s + 1)$
4	$(1.0552s^2 + 0.4889s + 1)(2.3213s^2 + 2.5522s + 1)$
5	$(2.136s + 1)(1.0406s^2 + 0.3196s + 1)(2.0115s^2 + 1.5614s + 1)$
6	$(1.7155s^2 + 1.06s + 1)(1.0313s^2 + 0.2376s + 1)(3.9963s^2 + 3.508s + 1)$
7	$(2.617s+1)(1.0241s^2+0.1765s+1)(1.5102s^2+0.7171s+1)(3.2679s^2+2.2825s+1)$
8	$(1.3927s^2 + 0.5411s + 1)(1.0195s^2 + 0.1405s + 1)(5.9688s^2 + 4.3832s + 1)(2.6116s^2 + 1.5684s + 1)$
9	$(3.07s+1)(1.3043s^2+0.4103s+1)(2.1574s^2+1.0724s+1)(1.0158s^2+0.1119s+1)(4.7851s^2 + 2.9606s + 1)$

B

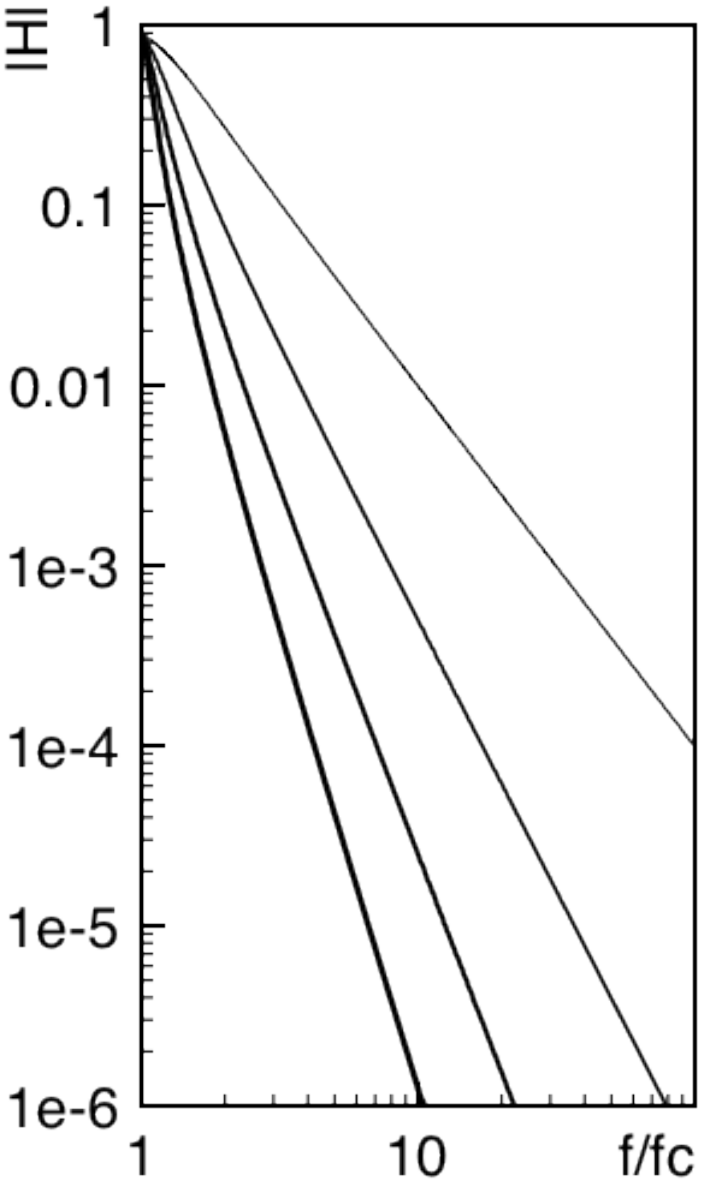
Frequency response of polynomial filters



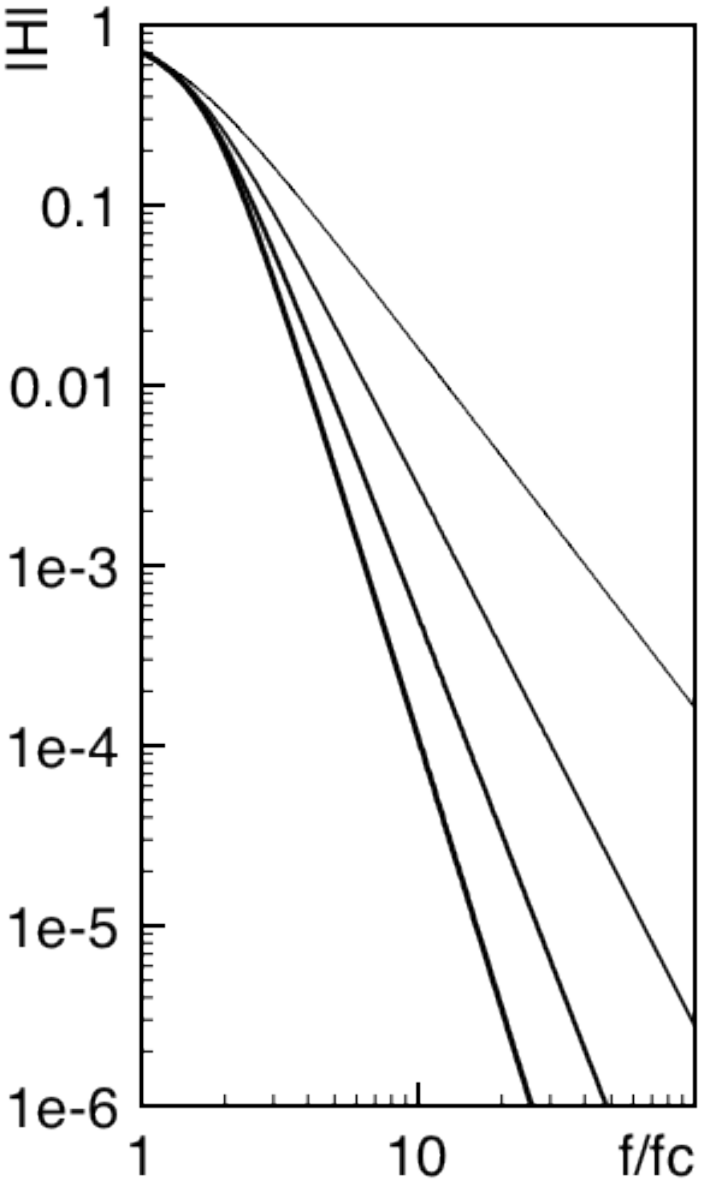
Butterworth low pass filter n = 2 to 5



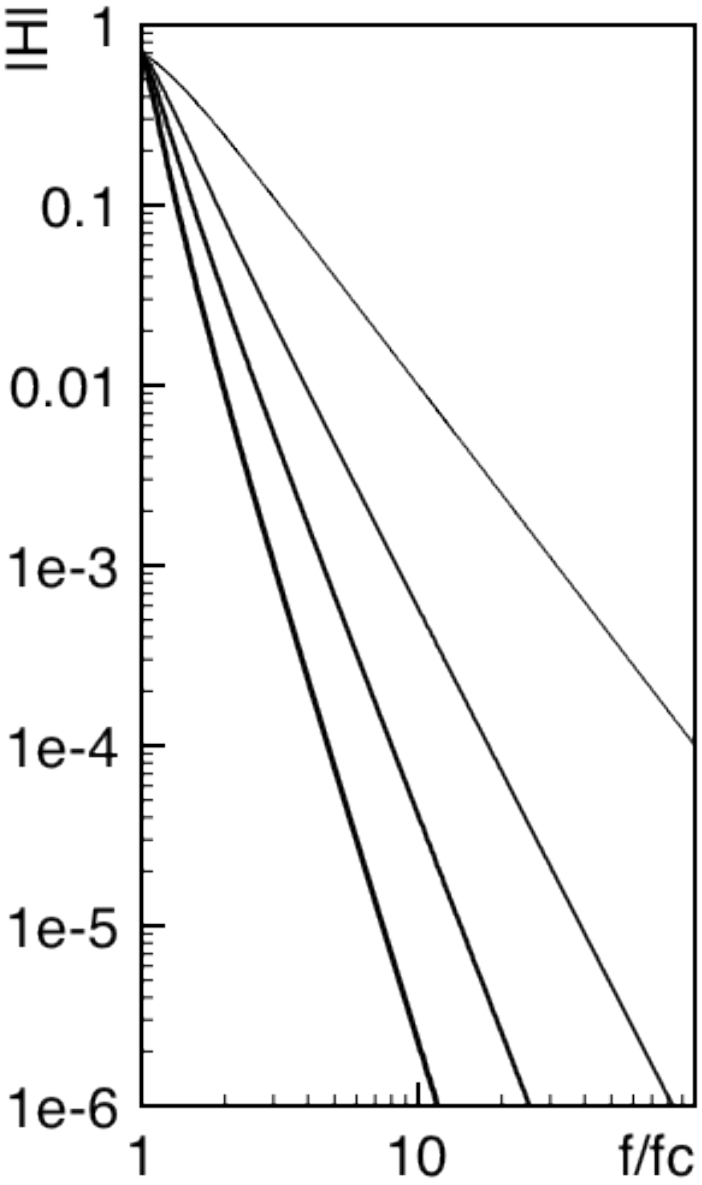
Chebishev 3dB low pass filter n = 2 to 5



Chebishev 1dB low pass filter n = 2 to 5



Bessel and Legendre low pass filter n = 2 to 5



Bessel and Legendre low pass filter n = 2 to 5

C

Angles, sin and cos transformation formulas

Basic trigonometric identities :

$\cos(-a) = \cos a$	$\sin(-a) = -\sin a$	$\tan(-a) = -\tan a$
$\cos(a+\pi) = -\cos a$	$\sin(a+\pi) = -\sin a$	$\tan(a+\pi) = \tan a$
$\cos(\pi - a) = -\cos a$	$\sin(\pi - a) = \sin a$	$\tan(\pi - a) = -\tan a$
$\cos\left(\frac{\pi}{2} + a\right) = -\sin a$	$\sin\left(\frac{\pi}{2} + a\right) = \cos a$	$\tan\left(\frac{\pi}{2} + a\right) = -1/\tan a$
$\cos\left(\frac{\pi}{2} - a\right) = \sin a$	$\sin\left(\frac{\pi}{2} - a\right) = \cos a$	$\tan\left(\frac{\pi}{2} - a\right) = 1/\tan a$

Sum and Difference of Angles :

$$\cos(a+b) = \cos a \times \cos b - \sin a \times \sin b \qquad \cos(a-b) = \cos a \times \cos b + \sin a \times \sin b$$
$$\sin(a+b) = \sin a \times \cos b + \cos a \times \sin b \qquad \sin(a-b) = \sin a \times \cos b - \cos a \times \sin b$$
$$\tan(a+b) = \frac{\tan a + \tan b}{1 - \tan a \times \tan b} \qquad \tan(a-b) = \frac{\tan a - \tan b}{1 + \tan a \times \tan b}$$

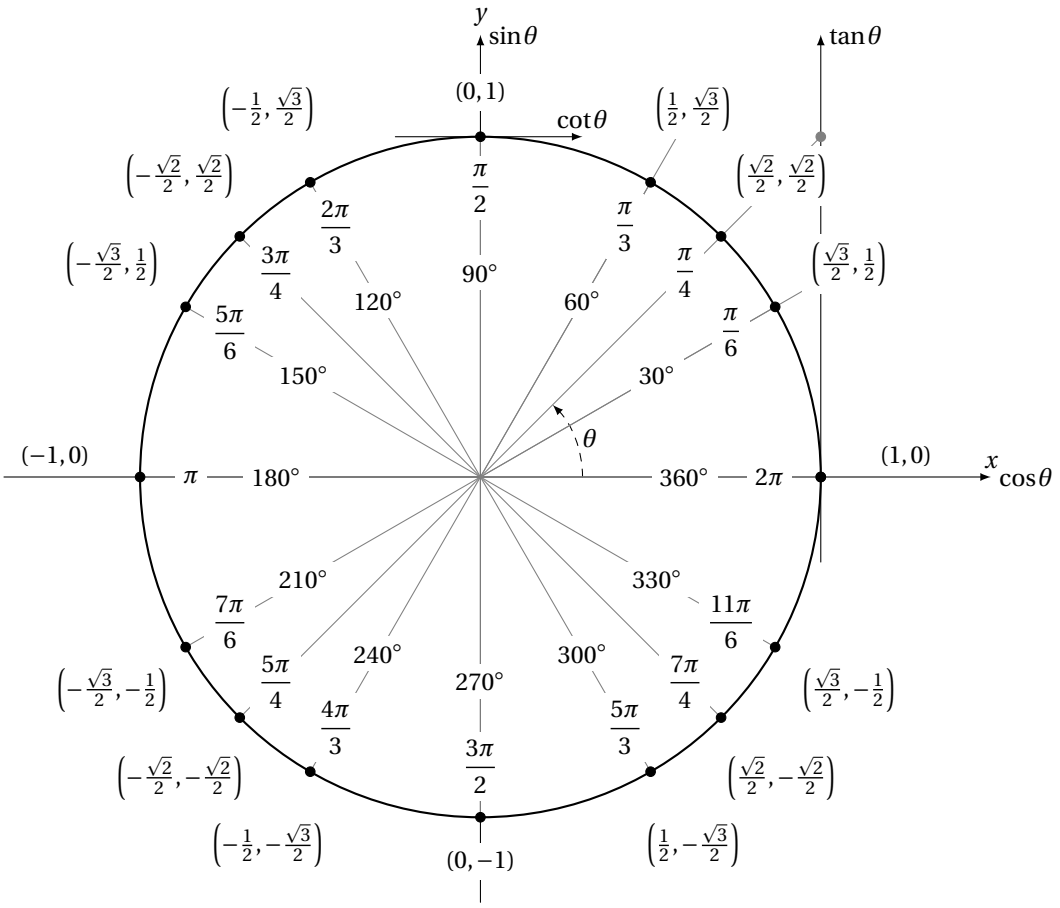
and for $a = b$:

$$\sin^2 a \times \cos^2 a = 1$$
$$\cos 2a = \cos^2 a - \sin^2 a = 2 \times \cos^2 a - 1 = 1 - 2 \times \sin^2 a$$
$$2 \times \cos^2 a = 1 + \cos 2a$$
$$2 \times \sin^2 a = 1 - \cos 2a$$
$$\sin 2a = 2 \times \sin a \times \cos a$$
$$\tan 2a = \frac{2 \times \tan a}{1 - \tan^2 a}$$

Multiplication of 2 Trigonometric Functions :

$$2 \times \cos a \times \cos b = (\cos(a+b) + \cos(a-b))$$
$$2 \times \sin a \times \sin b = (\cos(a-b) - \cos(a+b))$$
$$2 \times \sin a \times \cos b = (\sin(a+b) + \sin(a-b))$$

Trigonometric circle :



- x coordinate is the cosine of the angle θ
- y coordinate is the sine of the angle θ
- $\sin\theta/\cos\theta = \tan\theta$ is the tangent of the angle θ
- $\cos\theta/\sin\theta = \cot\theta$ is the cotangent of the angle θ

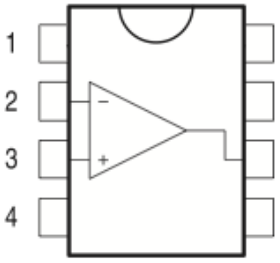


TL081 Data Sheet

TL081 GENERAL PURPOSE J-FET SINGLE OPERATIONAL AMPLIFIERS

- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- HIGH SLEW RATE : 16V/μs (typ)

PIN CONNECTIONS (top view)



1 - Offset null 1
2 - Inverting input
3 - Non-inverting
4 - V_{CC}^-
5 - Offset null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

DESCRIPTION

The TL081, TL081A and TL081B are high speed J–FET input single operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

ORDER CODE

Part Number	Temperature Range
TL081M/AM/BM	-55°C, +125°C
TL081I/AI/BI	-40°C, +105°C
TL081C/AC/BC	0°C, +70°C
Example : TL081CD, TL081IN	

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	M, AM, BM	TL081I, AI, BI	C, AC, BC	Unit
V_{CC}	Supply voltage - note 1)	±18			V
V_i	Input Voltage - note 2)	±15			V
V_{id}	Differential Input Voltage - note 3)	±30			V
P_{tot}	Power Dissipation	680			mW
	Output Short-circuit Duration - note 4)	Infinite			
T_{oper}	Operating Free-air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150			°C

ELECTRICAL CHARACTERISTICS

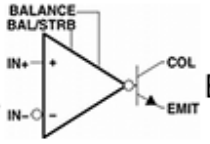
$V_{CC} = \pm 15V$, $T_{amb} = +25°C$

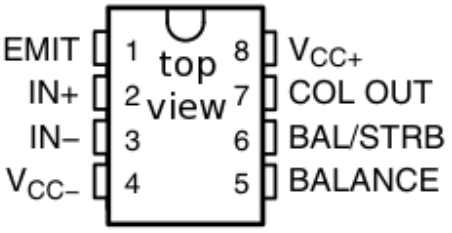
Symbol	Parameter		TL081I,M,AC,AI,AM, BC,BI,BM			TL081C		Unit
			Min.	Typ.	Max.	Min.	Typ.	
$\pm V_{opp}$	Output Voltage Swing							V
	$T_{amb} = +25°C$	RL = 2kΩ	10	12		10	12	
		RL = 10kΩ	12	13.5		12	13.5	
	$T_{min} \le T_{amb} \le T_{max}$	RL = 2kΩ	10			10		
		RL = 10kΩ	12			12		
SR	Slew Rate ($T_{amb} = +25°C$) $V_{in} = 10V$, $R_L = 2k\Omega$, $C_L = 100pF$, unity gain		8	16		8	16	V/µs
GBP	Gain Bandwidth Product ($T_{amb} = +25°C$) $V_{in} = 10mV$, $R_L = 2k\Omega$, $C_L = 100pF$, f= 100kHz		2.5	4		2.5	4	MHz
R_i	Input Resistance			10^{12}			10^{12}	Ω
e_n	Equivalent Input Noise Voltage $R_S = 100\Omega$, f = 1KHz			15			15	$\frac{nV}{\sqrt{Hz}}$

LM311
Comparator

The LM311 series is a monolithic, low input current voltage comparator. The device is also designed to operate from dual or single supply voltage.

- Low input bias current : 250nA (Max)
- Low input offset current : 50nA (Max)
- Differential Input Voltage : ±30V
- Power supply voltage : single 5.0V to ±15V
- Offset voltage null capability.





Absolute Maximum Ratings

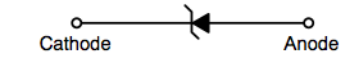
Parameter	Symbol	Value	Unit
Total Supply Voltage	V_{CC}	36	V
Output to Negative Supply Voltage LM311	V_O - V_{EE}	40	V
Ground to Negative voltage	V_{EE}	-30	V
Differential Input Voltage	$V_{I(DIFF)}$	30	V
Input Voltage	V_I	±15	V

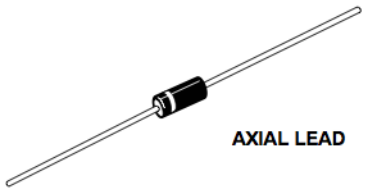
Electrical Characteristics

(V_{CC} = 15V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Voltage Gain	G_V		40	200	-	V/mV
Response Time	T_{RES}		-	200	-	ns
Saturation Voltage	V_{SAT}	I_O =50mA, $V_I \le$ -10mV	-	0.75	1.5	V
		$V_{CC} \ge$ 4.5V, V_{EE} =0V I_O =8mA, $V_I \le$ -10mV,	-	0.23	0.4	

Zener Voltage Regulators



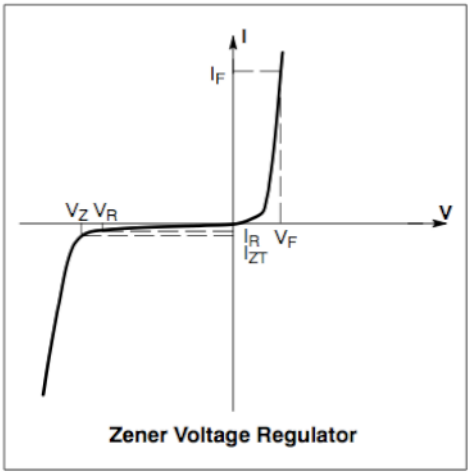


Features

- Zener Voltage Range – 3.3 V to 200 V
- ESD Rating of Class 3 (>16 kV) per Human Body Model
- Surge Rating of up to 180 W @ 8.3 ms
- Maximum Limits Guaranteed on up to Six Electrical Parameters
- Pb–Free Packages are Available*

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, V_F = 1.2 V Max @ I_F = 1.0 A for all types)

Symbol	Parameter
V_Z	Reverse Zener Voltage @ I_{ZT}
I_{ZT}	Reverse Current
Z_{ZT}	Maximum Zener Impedance @ I_{ZT}
I_{ZK}	Reverse Current
Z_{ZK}	Maximum Zener Impedance @ I_{ZK}
I_R	Reverse Leakage Current @ V_R
V_R	Breakdown Voltage
I_F	Forward Current
V_F	Forward Voltage @ I_F
I_R	Maximum Surge Current @ T_A = 25°C
ΔV_Z	Reverse Zener Voltage Change
I_{ZM}	Maximum DC Zener Current



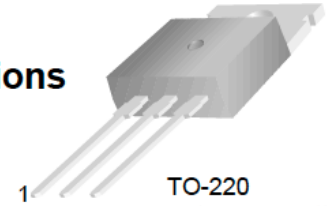
Zener Voltage Regulator

BDX54 Data Sheet

BDX54/A/B/C

- Power Darlington TR
- Complement to BDX53

Hammer Drivers, Audio Amplifiers Applications
Power Liner and Switching Applications



1
1.Base 2.Collector 3.Emitter

TO-220

PNP Epitaxial Silicon Transistor

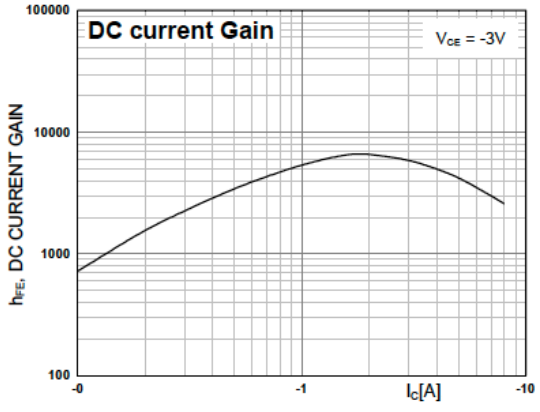
Absolute Maximum Ratings T_C=25°C unless otherwise noted

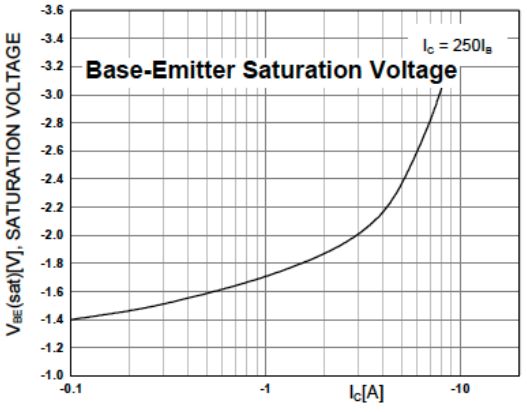
Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage : BDX54	- 45	V
V_{CEO}	Collector-Emitter Voltage : BDX54	- 45	V
V_{EBO}	Emitter-Base Voltage	- 5	V
I_C	Collector Current (DC)	- 8	A
I_{CP}	*Collector Current (Pulse)	- 12	A
I_B	Base Current	- 0.2	A

Electrical Characteristics T_C=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
I_{EBO}	Emitter Cut-off Current	V_{EB} = - 5V, I_C = 0		- 2	mA
h_{FE}	* DC Current Gain	V_{CE} = - 3V, I_C = - 3A	750		

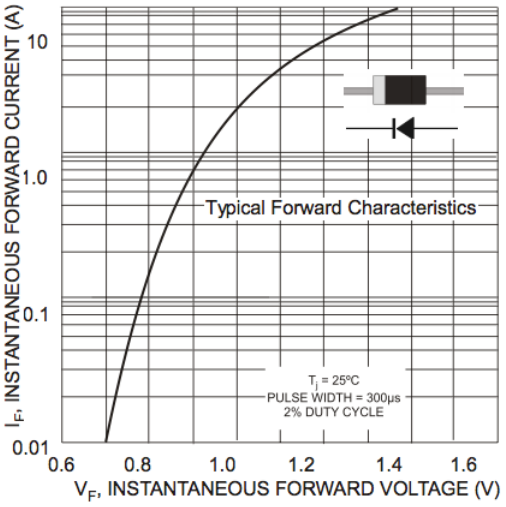
* Pulse Test: PW=300μs, duty Cycle =1.5% Pulsed





1N4001 THRU 1N4007

GENERAL PURPOSE SILICON RECTIFIER
VOLTAGE RANGE 50 TO 1000 Volts Current 1 Ampere



FEATURES

- Low forward voltage drop
- High current capability
- High reliability
- High surge current capability
- Exceeds environmental standards of MIL-S-19500/228

ELECTRICAL CHARACTERISTICS*

Rating	Symbol	Typ	Max	Unit
Maximum Instantaneous Forward Voltage Drop, (i_F = 1.0 Amp, T_J = 25°C)	v_F	0.93	1.1	V
Maximum Full–Cycle Average Forward Voltage Drop, (I_O = 1.0 Amp, T_L = 75°C, 1 inch leads)	$V_{F(AV)}$	–	0.8	V
Maximum Reverse Current (rated DC voltage) (T_J = 25°C) (T_J = 100°C)	I_R	 0.05 1.0	 10 50	μA
Maximum Full–Cycle Average Reverse Current, (I_O = 1.0 Amp, T_L = 75°C, 1 inch leads)	$I_{R(AV)}$	–	30	μA

MAXIMUM RATINGS

Rating	Symbol	1N4001	1N4002	1N4003	1N4004	1N4005	1N4006	1N4007	Unit
*Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	V
*Non–Repetitive Peak Reverse Voltage (halfwave, single phase, 60 Hz)	V_{RSM}	60	120	240	480	720	1000	1200	V
*RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	280	420	560	700	V
*Average Rectified Forward Current (single phase, resistive load, 60 Hz, T_A = 75°C)	I_O	1.0							A
*Non–Repetitive Peak Surge Current (surge applied at rated load conditions)	I_{FSM}	30 (for 1 cycle)							A
Operating and Storage Junction Temperature Range	T_J T_{stg}	–65 to +175							°C

I

LM158 Data Sheet

LM158 Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

Absolute Maximum Ratings

Supply Voltage, V^+	32V
Differential Input Voltage	32V
Input Voltage	−0.3V to +32V

Electrical Characteristics

Parameter	Conditions	Min	Typ
Large Signal Voltage Gain	V^+ = 15V, T_A = 25°C, $R_L \geq 2$ kΩ, (For V_O = 1V to 11V)	50	100

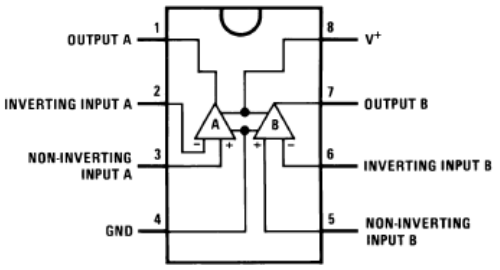
Advantages

- Two internally compensated op amps
- Eliminates need for dual supplies
- Allows direct sensing near GND and V_{OUT} also goes to GND

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain: 100 dB
- Wide bandwidth (unity gain): 1 MHz
- Wide power supply range:
  — Single supply: 3V to 32V
  — or dual supplies: ±1.5V to ±16V
- Very low supply current drain (500 µA)—essentially independent of supply voltage
- Low input offset voltage: 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing

DIP/SO Package



CD4046BC Micropower Phase-Locked Loop

General Description

The CD4046BC micropower phase-locked loop (PLL) consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two phase comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

Phase comparator I, an exclusive OR gate, provides a digital error signal (phase comp. I Out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II Out) and lock-in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

The linear voltage-controlled oscillator (VCO) produces an output signal (VCO Out) whose frequency is determined by the voltage at the VCO_{IN} input, and the capacitor and resistors connected to pin $C1_A$, $C1_B$, R1 and R2.

The source follower output of the VCO_{IN} (demodulator Out) is used with an external resistor of 10 kΩ or more.

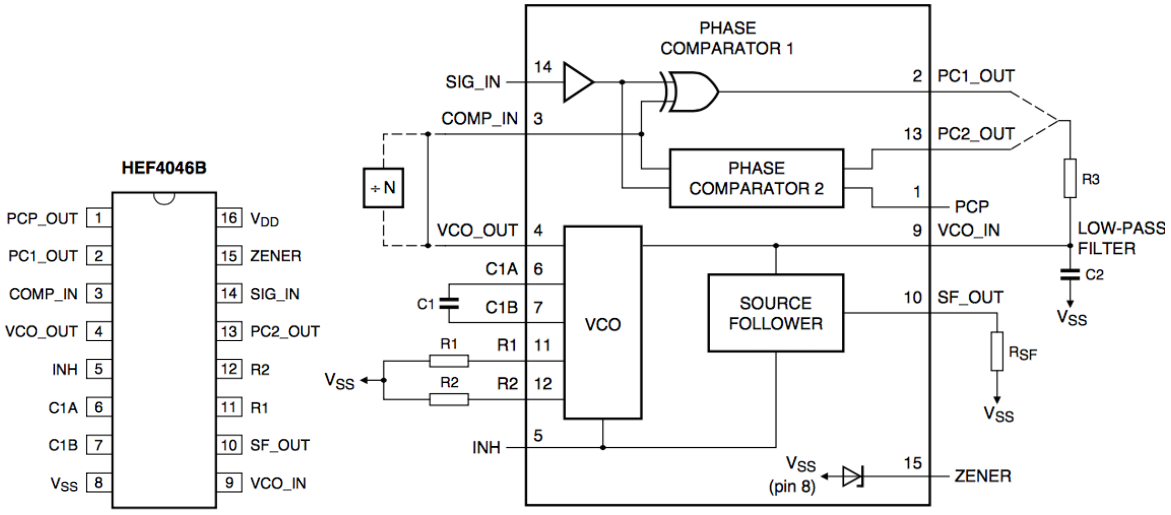
The INHIBIT input, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode is provided for power supply regulation, if necessary.

Features

- Wide supply voltage range: 3.0V to 18V
- Low dynamic power consumption: 70 µW (typ.) at f_o = 10 kHz, V_{DD} = 5V
- VCO frequency: 1.3 MHz (typ.) at V_{DD} = 10V
- Low frequency drift: 0.06%/°C at V_{DD} = 10V with temperature
- High VCO linearity: 1% (typ.)

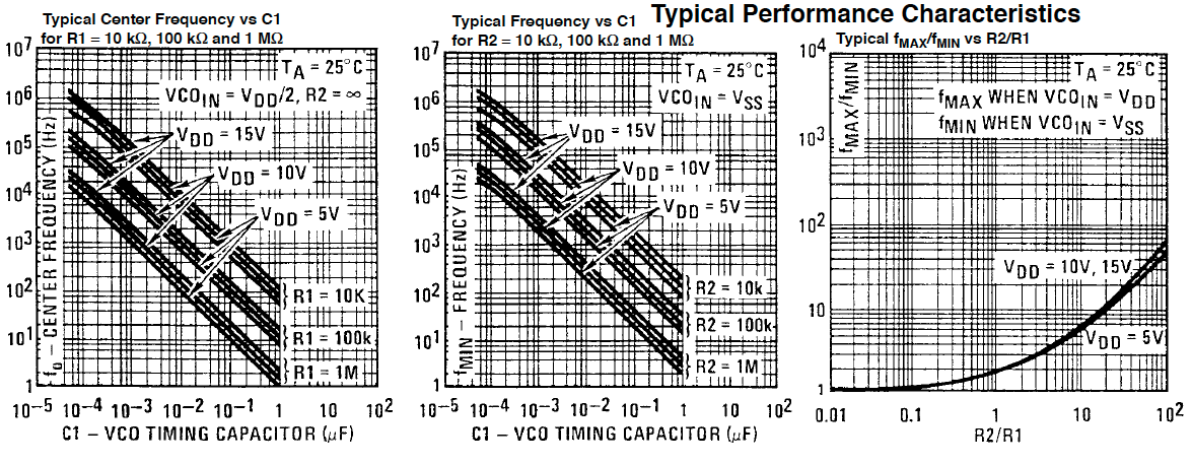
Applications

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discrimination
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Tone decoding
- FSK modulation
- Motor speed control

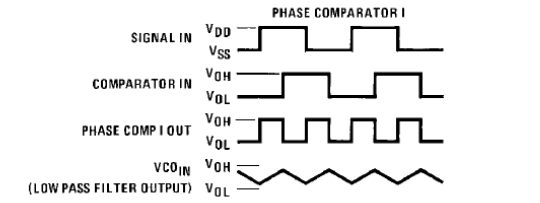


Symbol	Pin	Description
PCP_OUT	1	phase comparator pulse output
PC1_OUT	2	phase comparator 1 output
COMP_IN	3	comparator input
VCO_OUT	4	VCO output
INH	5	inhibit input
C1A	6	capacitor C1 connection A
C1B	7	capacitor C1 connection B
V_{SS}	8	ground supply voltage
VCO_IN	9	VCO input
SF_OUT	10	source-follower output
R1	11	resistor R1 connection
R2	12	resistor R2 connection
PC2_OUT	13	phase comparator 2 output
SIG_IN	14	signal input
ZENER	15	Zener diode input for regulated supply
V_{DD}	16	supply voltage

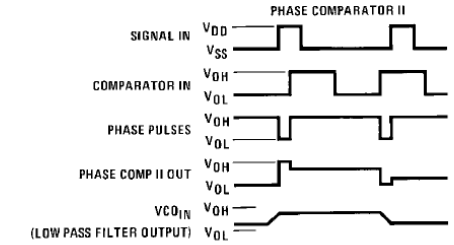
Typical Performance Characteristics



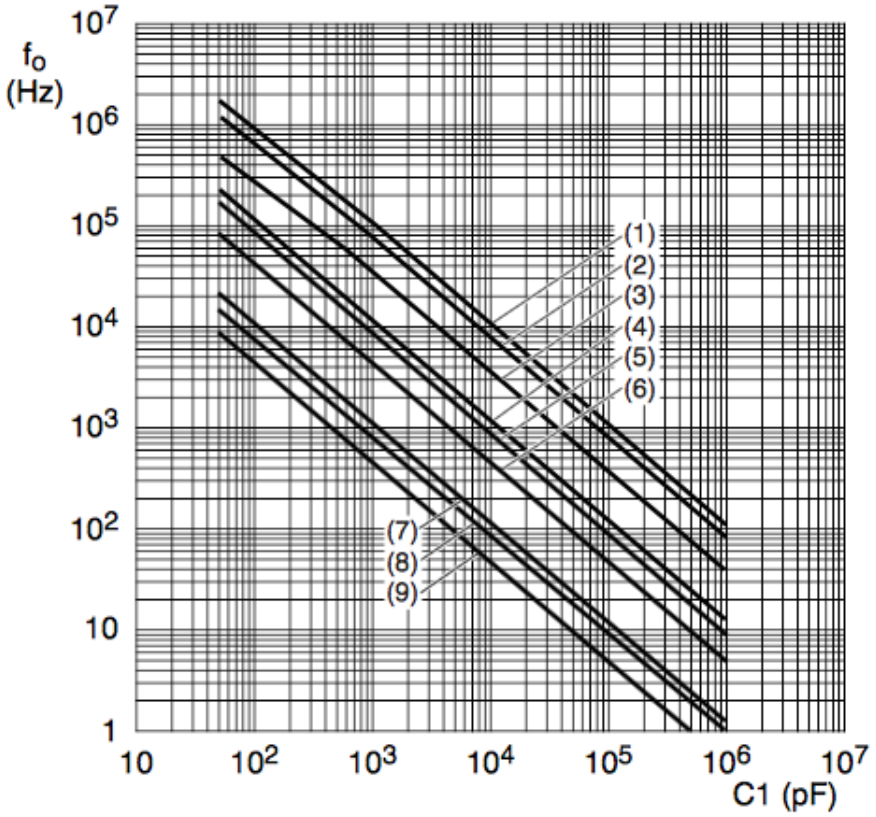
Typical Waveforms



Typical Waveform Employing Phase Comparator I in Locked Condition



Typical Waveform Employing Phase Comparator II in Locked Condition



T_{amb} = 25 °C; VCO_IN at $0.5V_{DD}$;
INH_IN at V_{SS}; R2 = ∞.

Lines (1), (4), and (7): V_{DD} = 15 V;

Lines (2), (5), and (8): V_{DD} = 10 V;

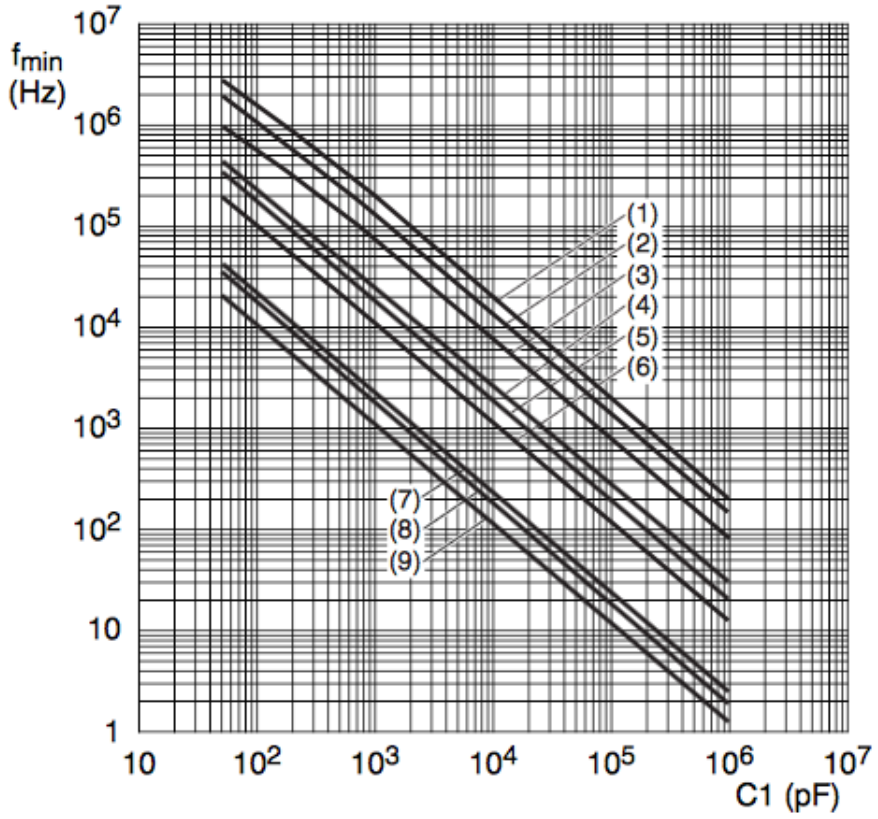
Lines (3), (6), and (9): V_{DD} = 5 V;

Lines (1), (2), and (3): R1 = 10 kΩ;

Lines (4), (5), and (6): R1 = 100 kΩ;

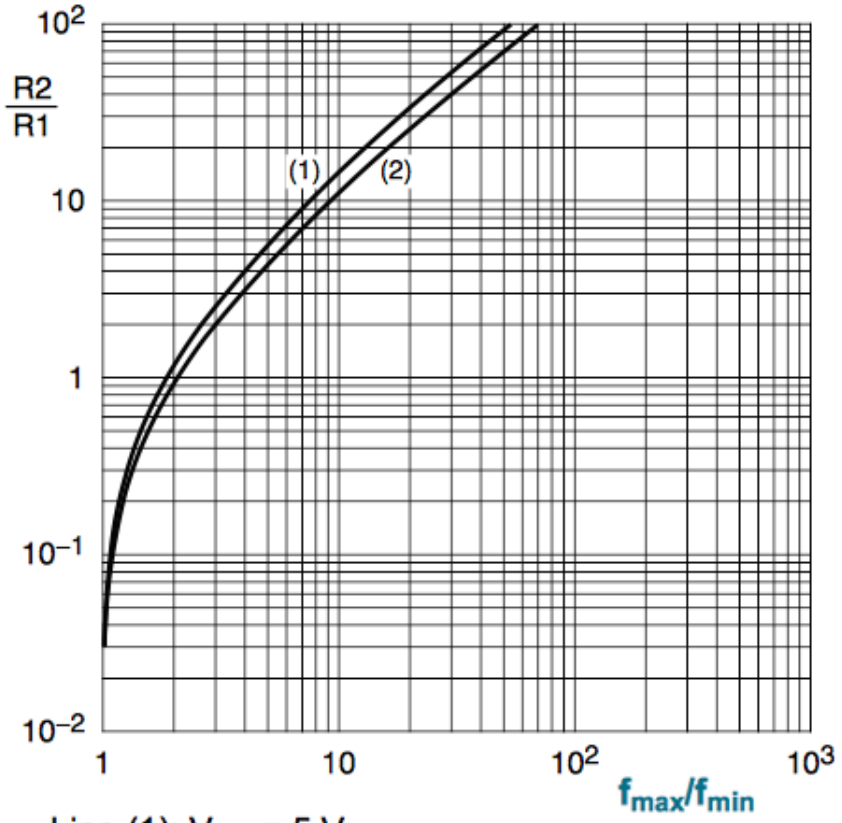
Lines (7), (8), and (9): R1 = 1 MΩ.

Typical center frequency as a function of capacitor C1



T_{amb} = 25 °C; VCO_IN at V_{SS}; INH_IN at V_{SS}; R1 = ∞.
Lines (1), (4), and (7): V_{DD} = 15 V;
Lines (2), (5), and (8): V_{DD} = 10 V;
Lines (3), (6), and (9): V_{DD} = 5 V;
Lines (1), (2), and (3): R2 = 10 kΩ;
Lines (4), (5), and (6): R2 = 100 kΩ;
Lines (7), (8), and (9): R2 = 1 MΩ.

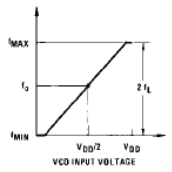
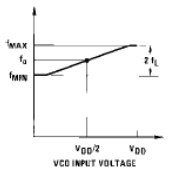
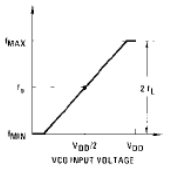
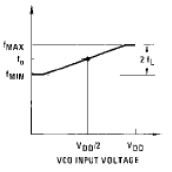
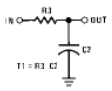
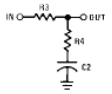
Typical frequency offset as a function of capacitor C1



Line (1): V_{DD} = 5 V;

Line (2): V_{DD} = 10 V, 15 V.

Typical ratio of R2/R1 as a function of the ratio f_{max}/f_{min}

Characteristics	Using Phase Comparator I		Using Phase Comparator II	
	VCO Without Offset R2 = ∞	VCO With Offset	VCO Without Offset R2 = ∞	VCO With Offset
VCO Frequency				
For No Signal Input	VCO in PLL system will adjust to center frequency, f_o		VCO in PLL system will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2f_L$	$2f_L$ = full VCO frequency range $2f_L = f_{max} - f_{min}$			
Frequency Capture Range, $2f_C$		$2f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$		
Loop Filter Component Selection		For $2f_C$, see Ref.		$f_C = f_L$
Phase Angle Between Single and Comparator	90° at center frequency (f_o), approximating 0° and 180° at ends of lock range ($2f_L$)		Always 0° in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	

Design Information

This information is a guide for approximating the value of external components for the CD4046B in a phase-locked-loop system. The selected external components must be within the following ranges: R1, R2 ≥ 10 kΩ, R_S ≥ 10 kΩ, C1 ≥ 50 pF.

In addition to the given design information, refer to Figure 5, Figure 6, Figure 7 for R1, R2 and C1 component selections.

Characteristics	Using Phase Comparator I		Using Phase Comparator II	
	VCO Without Offset R2 = ∞	VCO With Offset	VCO Without Offset R2 = ∞	VCO With Offset
VCO Component Selection	Given: f_o. Use f_o with Figure 5 to determine R1 and C1.	Given: f_o and f_L. Calculate f_{min} from the equation $f_{min} = f_o - f_L$. Use f_{min} with Figure 6 to determine R2 and C1. Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$. Use $\frac{f_{max}}{f_{min}}$ with Figure 7 to determine ratio R2/R1 to obtain R1.	Given: f_{max}. Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$. Use f_o with Figure 5 to determine R1 and C1.	Given: f_{min} and f_{max}. Use f_{min} with Figure 6 to to determine R2 and C1. Calculate $\frac{f_{max}}{f_{min}}$ Use $\frac{f_{max}}{f_{min}}$ with Figure 7 to determine ratio R2/R1 to obtain R1.

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CD4018 Data Sheet

CMOS Presettable Divide-By-'N' Counter

High-Voltage Types (20-Volt Rating)

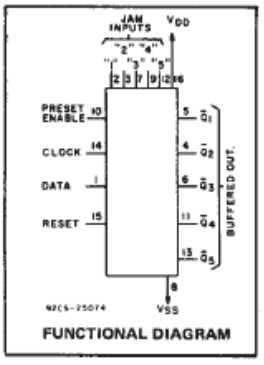
■ CD4018B types consist of 5 Johnson-Counter stages, buffered Q outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\overline{Q}5$, $\overline{Q}4$, $\overline{Q}3$, $\overline{Q}2$, $\overline{Q}1$ signals, respectively, back to the DATA input. Divide-by-9, 7, 5; or 3 counter configurations can be implemented by the use of a CD4011B to gate the feedback connection to the DATA input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018B units. The counter is advanced one count at the positive clock-signal transition. Schmitt Trigger action on the clock line permits unlimited clock rise and fall times. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

The CD4018B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

CD4018B Types

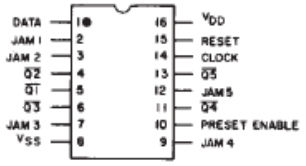
Features:

- **Medium speed operation . . . . . 10 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V**
- **Fully static operation**
- **100% tested for quiescent current at 20 V**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) = 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V**
- **Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM

TERMINAL DIAGRAM
Top View

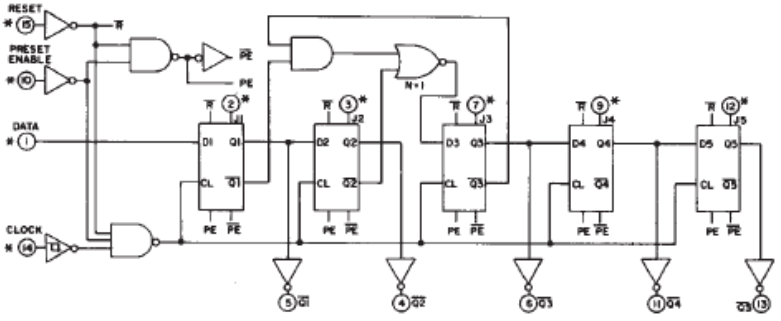


Applications:

- **Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters**
- **Fixed and programmable counters greater than 10**
- **Programmable decade counters**
- **Divide-by-"N" counters/frequency synthesizers**
- **Frequency division**
- **Counter control/timers**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA



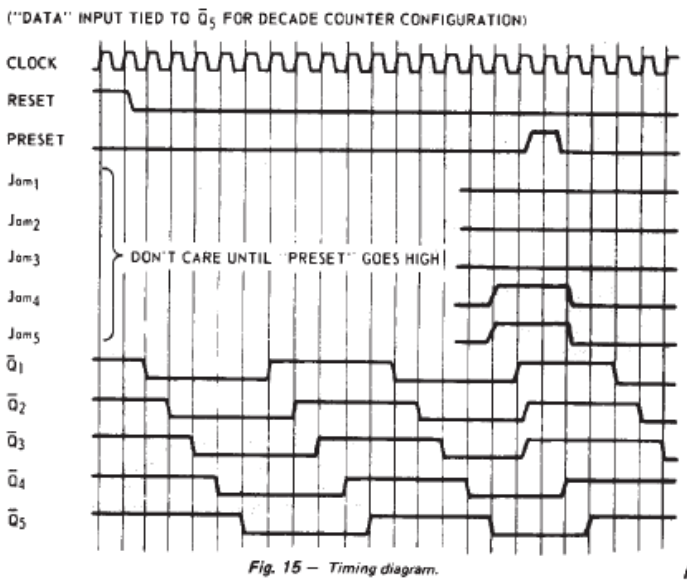


Fig. 15 — Timing diagram.

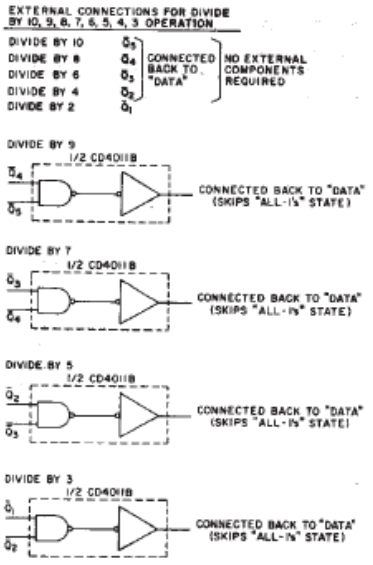


Fig. 16 — External connections for divide by 10, 9, 8, 7, 5, 4, 3, 2 operation.

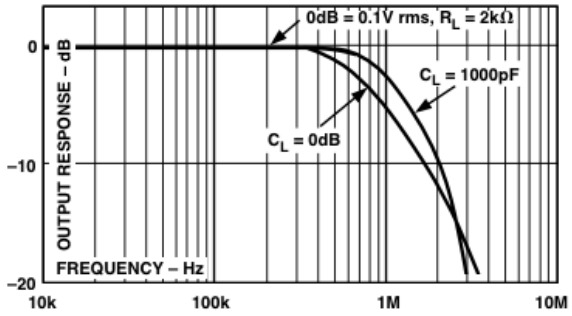
AD633 Analog Multiplier

PRODUCT DESCRIPTION

The AD633 is a functionally complete, four-quadrant, analog multiplier. It includes high impedance, differential X and Y inputs and a high impedance summing input (Z). The low impedance output voltage is a nominal 10 V full scale provided by a buried Zener. The AD633 is the first product to offer these features in modestly priced 8-lead plastic DIP and SOIC packages.

The AD633 is laser calibrated to a guaranteed total accuracy of 2% of full scale. Nonlinearity for the Y-input is typically less than 0.1% and noise referred to the output is typically less than 100 μV rms in a 10 Hz to 10 kHz bandwidth. A 1 MHz bandwidth, 20 V/μs slew rate, and the ability to drive capacitive loads make the AD633 useful in a wide variety of applications where simplicity and cost are key concerns.

The AD633's versatility is not compromised by its simplicity. The Z-input provides access to the output buffer amplifier, enabling the user to sum the outputs of two or more multipliers, increase the multiplier gain, convert the output voltage to a current, and configure a variety of applications.



FEATURES

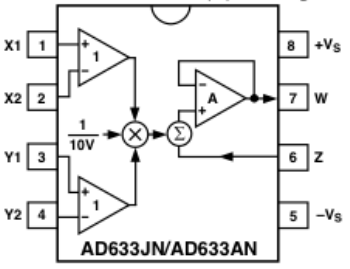
Four-Quadrant Multiplication
Low Cost 8-Lead Package
Complete—No External Components Req
Laser-Trimmed Accuracy and Stability
Total Error Within 2% of FS
Differential High Impedance X and Y Inputs
High Impedance Unity-Gain Summing Input
Laser-Trimmed 10 V Scaling Reference

APPLICATIONS

Multiplication, Division, Squaring
Modulation/Demodulation, Phase Detection
Voltage-Controlled Amplifiers/Attenuators/ Filters

CONNECTION DIAGRAMS

8-Lead Plastic DIP (N) Package



$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z$$

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . 500 mW
Input Voltages[3] . . . . . ±18 V
Output Short Circuit Duration . Indefinite

TRANSFER FUNCTION		$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10\ V} + Z$			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
MULTIPLIER PERFORMANCE					
Total Error	−10 V ≤ X, Y ≤ +10 V		±1	**±2**	% Full Scale
T_{MIN} to T_{MAX}			±3		% Full Scale
Scale Voltage Error	SF = 10.00 V Nominal		±0.25%		% Full Scale
Supply Rejection	V_S = ±14 V to ±16 V		±0.01		% Full Scale
Nonlinearity, X	X = ±10 V, Y = +10 V		±0.4	**±1**	% Full Scale
Nonlinearity, Y	Y = ±10 V, X = +10 V		±0.1	**±0.4**	% Full Scale
X Feedthrough	Y Nulled, X = ±10 V		±0.3	**±1**	% Full Scale
Y Feedthrough	X Nulled, Y = ±10 V		±0.1	**±0.4**	% Full Scale
Output Offset Voltage			±5	**±50**	mV
DYNAMICS					
Small Signal BW	V_O = 0.1 V rms		1		MHz
Slew Rate	V_O = 20 V p-p		20		V/μs
Settling Time to 1%	Δ V_O = 20 V		2		μs
OUTPUT NOISE					
Spectral Density			0.8		$\mu V/\sqrt{Hz}$
Wideband Noise	f = 10 Hz to 5 MHz		1		mV rms
	f = 10 Hz to 10 kHz		90		μV rms
OUTPUT					
Output Voltage Swing		**±11**			V
Short Circuit Current	R_L = 0 Ω		30	**40**	mA
INPUT AMPLIFIERS					
Signal Voltage Range	Differential	**±10**			V
	Common Mode	**±10**			V
Offset Voltage X, Y			±5	**±30**	mV
CMRR X, Y	V_{CM} = ±10 V, f = 50 Hz	**60**	80		dB
Bias Current X, Y, Z			0.8	**2.0**	μA
Differential Resistance			10		MΩ

FUNCTIONAL DESCRIPTION

The AD633 is a low cost multiplier comprising a translinear core, a buried Zener reference, and a unity gain connected output amplifier with an accessible summing node. Figure 1 shows the functional block diagram. The differential X and Y inputs are converted to differential currents by voltage-to-current converters. The product of these currents is generated by the multiplying core. A buried Zener reference provides an overall scale factor of 10 V. The sum of (X × Y)/10 + Z is then applied to the output amplifier. The amplifier summing node Z allows the user to add two or more multiplier outputs, convert the output voltage to a current, and configure various analog computational functions.

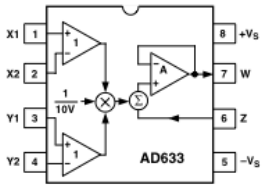


Figure 1. Functional Block Diagram (AD633JN Pinout Shown)

Inspection of the block diagram shows the overall transfer function to be:

$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10\ V} + Z \qquad \text{(Equation 1)}$$

ERROR SOURCES

Multiplier errors consist primarily of input and output offsets, scale factor error, and nonlinearity in the multiplying core. The input and output offsets can be eliminated by using the optional trim of Figure 2. This scheme reduces the net error to scale factor errors (gain error) and an irreducible nonlinearity component in the multiplying core. The X and Y nonlinearities are typically 0.4% and 0.1% of full scale, respectively. Scale factor error is typically 0.25% of full scale. The high impedance Z input should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise, the differential X and Y inputs should be referenced to their respective grounds to realize the full accuracy of the AD633.

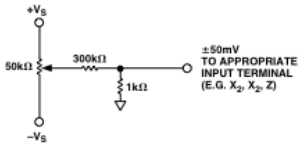


Figure 2. Optional Offset Trim Configuration

APPLICATIONS

The AD633 is well suited for such applications as modulation and demodulation, automatic gain control, power measurement, voltage controlled amplifiers, and frequency doublers. Note that these applications show the pin connections for the AD633JN pinout (8-lead DIP), which differs from the AD633JR pinout (8-lead SOIC).

Multiplier Connections

Figure 3 shows the basic connections for multiplication. The X and Y inputs will normally have their negative nodes grounded, but they are fully differential, and in many applications the grounded inputs may be reversed (to facilitate interfacing with signals of a particular polarity, while achieving some desired output polarity) or both may be driven.

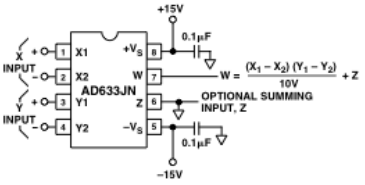


Figure 3. Basic Multiplier Connections

Squaring and Frequency Doubling

As Figure 4 shows, squaring of an input signal, E, is achieved simply by connecting the X and Y inputs in parallel to produce an output of $E^2/10$ V. The input may have either polarity, but the output will be positive. However, the output polarity may be reversed by interchanging the X or Y inputs. The Z input may be used to add a further signal to the output.

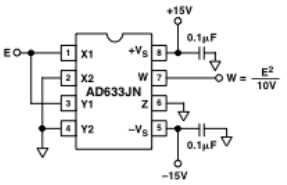


Figure 4. Connections for Squaring

When the input is a sine wave E sin ωt, this squarer behaves as a frequency doubler, since

$$\frac{(E \sin \omega t)^2}{10\ V} = \frac{E^2}{20\ V}(1 - \cos 2\,\omega t) \qquad \text{(Equation 2)}$$

Equation 2 shows a dc term at the output which will vary strongly with the amplitude of the input, E. This can be avoided using the connections shown in Figure 5, where an RC network is used to generate two signals whose product has no dc term. It uses the identity:

$$\cos\theta \sin\theta = \frac{1}{2}(\sin 2\,\theta) \qquad \text{(Equation 3)}$$

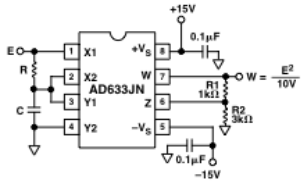


Figure 5. "Bounceless" Frequency Doubler

At $\omega_o = 1/CR$, the X input leads the input signal by 45° (and is attenuated by $\sqrt{2}$), and the Y input lags the X input by 45° (and is also attenuated by $\sqrt{2}$). Since the X and Y inputs are 90° out of phase, the response of the circuit will be (satisfying Equation 3):

$$W = \frac{1}{(10\,V)}\frac{E}{\sqrt{2}}\left(\sin \omega_o t + 45°\right)\frac{E}{\sqrt{2}}\left(\sin \omega_o t - 45°\right)$$

$$= \frac{E^2}{(40\,V)}\left(\sin 2\ \omega_o t\right) \qquad \text{(Equation 4)}$$

which has no dc component. Resistors R1 and R2 are included to restore the output amplitude to 10 V for an input amplitude of 10 V.

The amplitude of the output is only a weak function of frequency: the output amplitude will be 0.5% too low at $\omega = 0.9\ \omega_o$, and $\omega_o = 1.1\ \omega_o$.

Generating Inverse Functions

Inverse functions of multiplication, such as division and square rooting, can be implemented by placing a multiplier in the feedback loop of an op amp. Figure 6 shows how to implement a square rooter with the transfer function

$$W = \sqrt{-(10\,V)E} \qquad \text{(Equation 5)}$$

for the condition E<0.

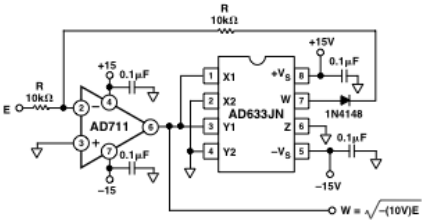


Figure 6. Connections for Square Rooting

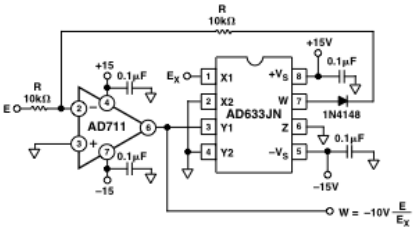


Figure 7. Connections for Division

Likewise, Figure 7 shows how to implement a divider using a multiplier in a feedback loop. The transfer function for the divider is

$$W = -(10\,V)\frac{E}{E_X} \qquad \text{(Equation 6)}$$

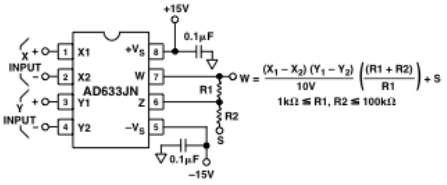


Figure 8. Connections for Variable Scale Factor

Variable Scale Factor

In some instances, it may be desirable to use a scaling voltage other than 10 V. The connections shown in Figure 8 increase the gain of the system by the ratio (R1 + R2)/R1. This ratio is limited to 100 in practical applications. The summing input, S, may be used to add an additional signal to the output or it may be grounded.

Current Output

The AD633's voltage output can be converted to a current output by the addition of a resistor R between the AD633's W and Z pins as shown in Figure 9 below. This arrangement forms

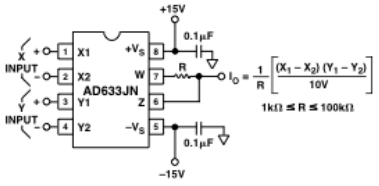


Figure 9. Current Output Connections

the basis of voltage controlled integrators and oscillators as will be shown later in this Applications section. The transfer function of this circuit has the form

$$I_O = \frac{1}{R}\frac{(X_1 - X_2)(Y_1 - Y_2)}{10\,V} \qquad \text{(Equation 7)}$$

Linear Amplitude Modulator

The AD633 can be used as a linear amplitude modulator with no external components. Figure 10 shows the circuit. The carrier and modulation inputs to the AD633 are multiplied to produce a double-sideband signal. The carrier signal is fed forward to the AD633's Z input where it is summed with the double-sideband signal to produce a double-sideband with carrier output.

Voltage Controlled Low-Pass and High-Pass Filters

Figure 11 shows a single multiplier used to build a voltage controlled low-pass filter. The voltage at output A is a result of filtering, E_S. The break frequency is modulated by E_C, the control input. The break frequency, f_2, equals

$$f_2 = \frac{E_C}{(20\,V)\pi\,RC} \qquad \text{(Equation 8)}$$

and the rolloff is 6 dB per octave. This output, which is at a high impedance point, may need to be buffered.

The voltage at output B, the direct output of the AD633, has same response up to frequency f_1, the natural breakpoint of RC filter,

$$f_1 = \frac{1}{2\,\pi\,RC} \qquad \text{(Equation 9)}$$

then levels off to a constant attenuation of $f_1/f_2 = E_C/10$.

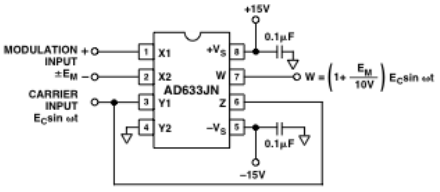


Figure 10. Linear Amplitude Modulator

For example, if R = 8 kΩ and C = 0.002 μF, then output A has a pole at frequencies from 100 Hz to 10 kHz for E_C ranging from 100 mV to 10 V. Output B has an additional zero at 10 kHz (and can be loaded because it is the multiplier's low impedance output). The circuit can be changed to a high-pass filter Z interchanging the resistor and capacitor as shown in Figure 12 below.

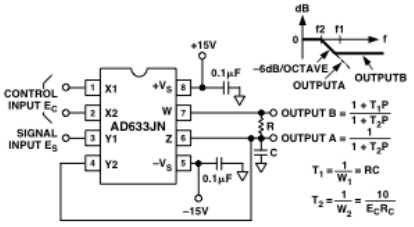


Figure 11. Voltage Controlled Low-Pass Filter

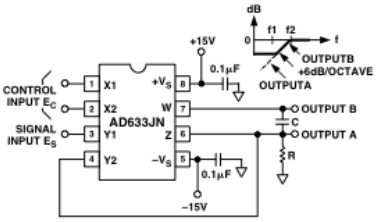


Figure 12. Voltage Controlled High-Pass Filter

Voltage Controlled Quadrature Oscillator

Figure 13 shows two multipliers being used to form integrators with controllable time constants in a 2nd order differential equation feedback loop. R2 and R5 provide controlled current output operation. The currents are integrated in capacitors C1 and C2, and the resulting voltages at high impedance are applied to the X inputs of the "next" AD633. The frequency control input, E_C, connected to the Y inputs, varies the integrator gains with a calibration of 100 Hz/V. The accuracy is limited by the Y-input offsets. The practical tuning range of this circuit is 100:1. C2 (proportional to C1 and C3), R3, and R4 provide regenerative feedback to start and maintain oscillation. The diode bridge, D1 through D4 (1N914s), and Zener diode D5 provide economical temperature stabilization and amplitude stabilization at ±8.5 V by degenerative damping. The output from the second integrator (10 V sin ωt) has the lowest distortion.

AGC AMPLIFIERS

Figure 14 shows an AGC circuit that uses an rms-dc converter to measure the amplitude of the output waveform. The AD633 and A1, 1/2 of an AD712 dual op amp, form a voltage controlled amplifier. The rms dc converter, an AD736, measures the rms value of the output signal. Its output drives A2, an integrator/comparator, whose output controls the gain of the voltage controlled amplifier. The 1N4148 diode prevents the output of A2 from going negative. R8, a 50 kΩ variable resistor, sets the circuit's output level. Feedback around the loop forces the voltages at the inverting and noninverting inputs of A2 to be equal, thus the AGC.

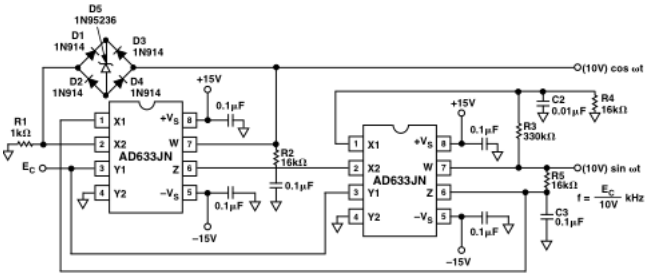


Figure 13. Voltage Controlled Quadrature Oscillator

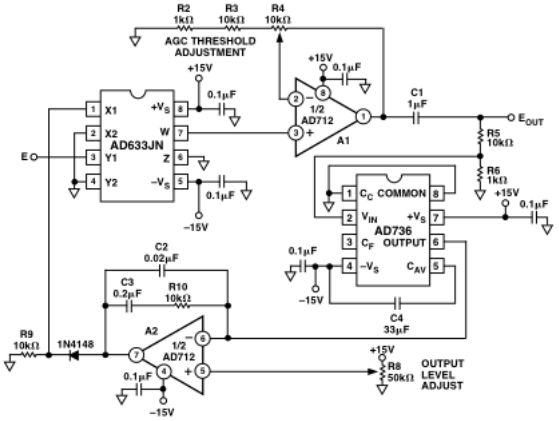


Figure 14. Connections for Use in Automatic Gain Control Circuit

M

Signal diode Data Sheet

High-speed diodes 1N4148

- Hermetically sealed leaded glass SOD27 (DO-35)
- High switching speed: max. 4 ns
- General application
- Continuous reverse voltage: max. 100 V
- Repetitive peak reverse voltage: max. 100 V
- Repetitive peak forward current: max. 450 mA.

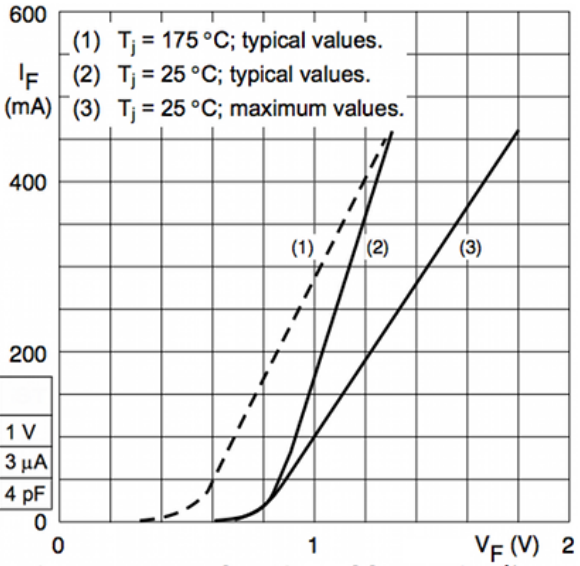
APPLICATIONS

- High-speed switching.



symbol

SYMBOL	MAX. ELECTRICAL CHARACTERISTICS		
V_F	forward voltage	I_F = 10 mA	1 V
I_R	reverse current	V_R = 20 V; T_j = 100 °C	3 µA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V	4 pF



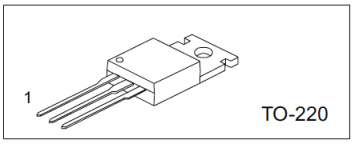
Forward current as a function of forward voltage.



78XX Linear voltage regulator Data Sheet

LM78XX LINEAR INTEGRATED CIRCUIT

3-TERMINAL 1A POSITIVE VOLTAGE REGULATOR



1:Input 2:GND 3:Output

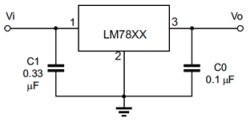
DESCRIPTION

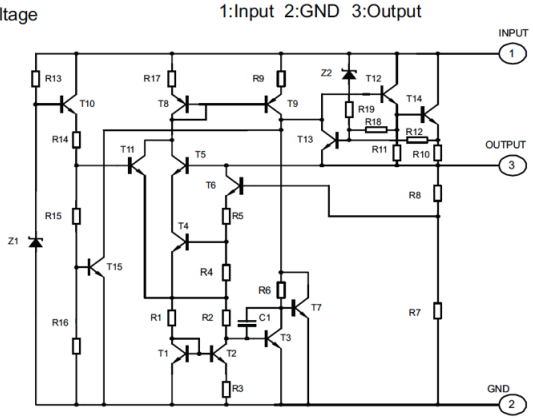
The Contek 78XX family is monolithic fixed voltage regulator integrated circuit. They are suitable for applications that required supply current up to 1 A.

FEATURES

*Output current up to 1.5 A
*Fixed output voltage of 5V, 6V, 8V, 9V, 10V, 12V, 15V ,18V and 24V available
*Thermal overload shutdown protection
*Short circuit current limiting
*Output transistor SOA protection

APPLICATION CIRCUIT





LM7805 ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage	Vo	Tj=25 C, Io=5mA - 1.0A	4.8	5.0	5.2	V
		VI =7.5V to 20V, Io=5mA - 1.0A,PD<15W	4.75		5.25	V
Load Regulation	ΔVo	Tj=25 C,Io=5mA - 1.5A			50	mV
		Tj=25 C,Io=0.25A - 0.75A			25	mV
Line regulation	ΔVo	VI =7V to 25V,Tj=25 C			50	mV
		VI =7.5V to 20V,Tj=25 C,Io=1A			50	mV
Quiescent Current	Iq	Tj=25 C, Io=<1A			8.0	mA
Quiescent Current Change	ΔIq	VI =7.5V to 20V			1.0	mA
	ΔIq	Io=5mA - 1.0A			0.5	mA
Output Noise Voltage	VN	10Hz<=f<=100kHz		40		μV
Temperature coefficient of Vo	ΔVo/ΔT	Io=5mA		-0.6		mV/ C
Ripple Rejection	RR	VI =8V - 18V,f=120Hz,Tj=25 C	62	80		dB
Peak Output Current	IPK	Tj=25 C		1.8		A
Short-Circuit Current	Isc	VI=35V, Tj=25 C		250		mA
Dropout Voltage	Vd	Tj=25 C		2.0		V