

ESSDERC/ESSCIRC 2008

Tutorial Session T2 on

Characterisation for the Nanoelectronics Era

Monday, 15 September 2008
Edinburgh, UK

Organized with the support of



Tutorial Organizers :
Prof. Anthony O'Neil
Newcastle University, UK
Prof. Herman E. Maes,
IMEC, Leuven, Belgium

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One of the objectives of the PULLNANO IP-project is to organize training sessions and courses to researchers and engineers in Europe, based on the know-how built up within this project.

The **ESSDERC/ESSCIRC 2008** conference has been considered to be a very suited forum for such a contribution from PULLNANO and more in particular in the area of characterisation of nanometer technologies and devices on which significant achievements were realized in the course of this project. The topics that were selected are related to very challenging issues in the development of nanometer technologies and devices. These include the characterisation of high-k materials, the characterisation of shallow junctions and the modeling and characterisation of stress and strain. We are pleased to offer a very exciting Tutorial program involving an elite group of lecturers who are experts in their field and also excellent teachers and who will give a general introduction in their area of competence complemented with results from the related research activities within PULLNANO.

This Tutorial session offers an excellent introduction to the relevant issues and is therefore strongly recommended and in fact a 'must' not only to those who start in this field but also to all physicists and engineers who want to get familiar with the characterisation issues in these nanometer devices.

We look forward to welcoming you in the Tutorial session in Edinburgh.

Anthony O'Neil, Newcastle University
Herman E. Maes, IMEC
Tutorial Chairmen

Program

Tutorial Session on **Nanoelectronics : Characterisation for the nanoelectronics era**

1.45pm-2.00pm	Welcome and Introduction to the Tutorial Session <i>Anthony O'Neil, Newcastle University, UK</i> <i>Herman E. Maes, IMEC, Leuven, Belgium</i>
2.00pm-2.45pm	Introducing Characterisation and Metrology <i>Tom Stevenson, University of Edinburgh, UK</i>
2.45pm-3.30pm	Physical Characterization of high-k materials <i>Christophe Wyon, STMicroelectronics, France</i>
3.30pm-4.00pm	Coffee Break
4.00pm-4.30pm	Two-dimensional Carrier Profile Characterization for junction engineering in advanced devices. <i>Pierre Eyben and W.Vandervorst, IMEC, Belgium</i>
4.30pm-5.15pm	Strain measurements in layers and devices <i>Alain Claverie, CEMES/CNRS, Groupe nMat, Toulouse, France</i>
5.15pm-6.00pm	Process simulation for advanced stress and junction engineering <i>Christophe Krzeminski and Evelyne Lampin, IEMN, France</i>
6.00pm	End of Session

Abstracts and CV's of the Lecturers

2.00-2.45pm

Introducing Characterisation and Metrology

Tom Stevenson

University of Edinburgh, UK

The tutorial will provide an introductory review of the major metrology techniques which are used in the microfabrication of devices on silicon, for both conventional circuits and MEMS devices.

When a layer of material is grown or deposited, process engineers need to monitor and control layer thickness, composition, stress, surface finish, and optical properties. The subsequent photolithography process has its own set of measurements including resist thickness, critical dimensions [CD] and layer to layer registration [overlay]. The etch process will again require CD measurement as well as layer thickness or etch depth.

As dimensions have shrunk on conventional devices, metrology techniques have had to change in order to resolve and measure the smaller features [CD] and thinner layers. On MEMS devices, the critical dimensions may still be relatively large and amenable to optical imaging but this approach may be difficult when layers are 10s or 100s of microns thick.

The tutorial will conclude by highlighting some of the major metrology challenges which are predicted by the roadmap.

Tom Stevenson is Operations Director of the Scottish Microelectronics Centre, University of Edinburgh, responsible for all aspects of cleanroom operations. He is also active, in a technical capacity, in a number of research areas, ranging from novel device structures to CMP for MEMS devices.

His interest in metrology dates back to 1969 when he studied Instrument Design at the University of Aberdeen [M.Sc.] and thereafter spent 5 years at Ferranti Ltd., Dalkeith as a development engineer on moire fringe measuring systems for machine tools and co-ordinate measuring machines.

At the University of Edinburgh, his main research interests have been in optical lithography and metrology associated with microfabrication of both microelectronic and MEMS devices.

2.45-3.30pm

Physical Characterization of high-k materials

Christophe Wyon

STMicroelectronics, France

In the frame of the European PullNano project, several techniques for the chemical and morphological characterization of advanced gate stacks, and in particular the high κ dielectric, have been investigated. Several practical aspects of Scanning Transmission Electron Microscopy- Electron Energy Loss Spectroscopy (STEM-EELS) and other TEM methods in the application to gate stacks were addressed. High κ / metal gate process was accurately characterized using Synchrotron Radiation- X-ray Photoelectron Spectroscopy (SR-XPS). SR-

XPS enables the characterization of buried thin films like interfacial layers, which usually occur in the high κ process.

The on-line monitoring of high κ related processes was successfully achieved using X-Ray Reflectivity (XRR) technique.

Christophe Wyon is manager of the ST Crolles Physical Characterization department since 2002. After receiving a PhD in Surface Physics and Chemistry from the National Polytechnique Institute of Grenoble, he joined CEA-LETI for working on crystal growth of dielectric materials. In 1990 he managed the crystal growth laboratory before taking the head of Thermal processes and wet chemistry in the Microelectronics Department in 1997. In 1999 Christophe Wyon was in charge of the Physical and Chemical Characterization laboratory at CEA-LETI.

Christophe Wyon led several European projects devoted to the physical and chemical characterization and metrology of advanced CMOS processes. He is author and co-author of more than 55 international papers.

4.00-4.30pm

Two-dimensional Carrier Profile Characterization for junction engineering in advanced devices.

*Pierre Eyben and W.Vandervorst
IMEC, Leuven, Belgium*

Junction engineering in advanced devices is a complex task as it requires a complete understanding of all possible 1D- and 2D interactions and the interplay between preamorphization steps, halo-implants and LDD/HDD profiles but equally the impact of (outdiffusion into) liners, details of the gate profile and implant tilt, pile-up during silicidation, stress effects on diffusion and activation etc...Due to this complexity simple 1D-experiments are no longer adequate and only true 2D-carrier (and dopant) profiles will provide the required fundamental understanding. The requirements on the characterization techniques for 2D-profiling are very stringent as one needs to combine sub-nm spatial resolution, with a high sensitivity (covering the entire concentration range of interest), and accurate quantification. Within the PULLNANO project Scanning Spreading Resistance Microscopy (SSRM) has emerged as the sole method able to fulfil all these requirements with a resolution as small as 0.5 nm. In this presentation we will discuss the basic aspects of SSRM, demonstrate its compliance with all (ITRS)-requirements and demonstrate its application for process development and TCAD calibration on planar and FINFET devices.

Pierre Eyben was born in 1975, obtained his Masters degree in Engineering in 1998 (Univ Liege) and in 2004 his Ph.D degree at the K.U.Leuven with a thesis titled “Scanning Spreading Resistance Microscopy : high resolution two-dimensional carrier profiling of semiconductor structures”. From 2004-2006 he worked as a post-doctoral fellow from the IWT (Flemish Institute for Science and Technology) at IMEC on the further implementation of SSRM and joined Imec in 2006 where he is now responsible for the SSRM research and service activities.

Wilfried Vandervorst was born in 1954, obtained his Master degree in Engineering in 1977 and Ph.D degree 1984 (K.U.Leuven). He joined IMEC in 1985 where he is presently heading the Materials and Components Analysis group. In 1990 he also became a professor at the K.U.Leuven and was nominated as Imec Fellow in 2001. His prime research is presently

focused on the development of metrology concepts for the characterization advanced devices with a special emphasis on approaches with high 2D/3D resolution.

4.30-5.15pm

Strain measurements in layers and devices

Alain Claverie

CEMES/CNRS, Groupe nMat, Toulouse, France

While stress in chips has been for long an undesirable effect resulting from processing and/or packaging, strained silicon is now an integral feature of the latest generation of transistors and electronic devices because of the associated enhancement in carrier mobility. Different strategies have been used to engineer strain in devices, leading to complex strain distributions in two and three dimensions. Developing methods of strain measurement at the nanoscale has therefore been an important objective in recent years but has proved elusive in practice: none of the existing techniques combines the necessary spatial resolution, precision and field of view. For example, Raman spectroscopy or X-ray diffraction techniques can map strain at the micrometer scale, whereas transmission electron microscopy allows strain measurement at the nanometer scale but only over small sample areas. Along this tutorial, we will review and discuss the applicability of these different techniques through technologically relevant examples and present a recently invented technique capable of bridging this gap and measuring strain to high precision, with nanometre spatial resolution and for micrometer fields of view.

Alain Claverie obtained the Dipl.-Ing. degree in Solid State Physics in 1981 from the National Institute for Applied Science (INSA) of Toulouse then his PhD in 1984 from the University Paul Sabatier of Toulouse. From 1985, he was Staff Scientist (permanent position) in the semiconductor group at CEMES, an autonomous laboratory of the National Center for Scientific Research, where he performed experimental work on TEM characterization of ion implanted materials. From 1988 to 1993, he has been visiting or staff scientist in national laboratories abroad, notably in India (Chandigarh) and California (Berkeley). Alain's interest ranges from the nucleation and growth of extended defects and nanoprecipitates, diffusion anomalies in semiconductors and very low energy ion implantation. He is the author or co-author of more than 150 publications in international journals and serves as a regular reviewer for APL, JAP, PRL, PR and Nature Materials. He has been the organizer of several international conferences (MRS (3), E-MRS (3), IEEE, GADEST...) and is a member of the scientific/technical boards of several others. Recently, he was the coordinator of the EC supported NEON (nanoparticles for electronics) a GROWTH Project aimed at engineering nanocrystals for memory applications. Appointed as "Directeur de Recherches" in 2002, he is now in the charge of "nanoMaterials Group" he created at CEMES where about 30 permanent scientists and about the same number of PhDs and PostDocs work on the synthesis, the physics, the characterization and the integration of nano-crystals and ultrathin films in systems for applications in electronics, magnetism and optics. Alain can be reached at claverie@cemes.fr

5.15-6.00pm

Process simulation for advanced stress and junction engineering

Christophe Krzeminski and Evelyne Lampin

IEMN, France

For CMOS devices downscaling, sharp requirements have been defined by the International Technology Roadmap for Semiconductors (ITRS) in terms of drive and off state current and power density, making the geometric scaling a challenging task. The new vector largely adopted to extend Moore's law is the mobility enhancement through the introduction of stress by several techniques (Stress Liner, eSiGe embedded stressor, stress memorization). On the other side, a challenging experimental trade-off is being made on junction processing to meet the sharp requirements in terms of resistance, abruptness and depth. Standard techniques (implantation and rapid thermal annealing) are being pushed to their limits whereas alternative techniques such as preamorphization, solid phase epitaxy (SPE), laser annealing and plasma doping are being optimized. As will be shown in this session of PULLNANO tutorials, many challenges are being faced by characterisation methods and metrology to support all of this intense research competition. TCAD more generally, and process simulation in particular, have a complementary role to play to identify trade-off and evaluate the scalability. The progresses recently made by standard finite element based simulators for the modeling of implantation, diffusion and stress engineering will be reviewed and illustrated by examples from different european projects and from the literature. Furthermore, as the complexity increases with device downscaling, atomistic simulations are of interest to provide more understanding and to perform computer experiments in cases where the time or atomic scale are very challenging for characterization. Several examples from our recent research work with molecular dynamics in PULLNANO will be presented.

Christophe Krzeminski was born in 1975. He received the Engineer degree from the "Institut Supérieur d'Electronique et du Numérique" in 1998 and the Ph.D. degree in electronics from the University of Lille, in 2001. From 1998 and 2001, he was involved with the modeling of electronic transport in molecular nanometric electronics devices. In 2001, he joined the institute d'Electronique, de Microelectronique et de Nanotechnologie (IEMN) as an Assistant Professeur in the Silicon Microelectronics Department. His research was first focused on the development of a new approach to silicon oxidation and oxynitridation modeling. In 2003, he joined the Centre de la Recherche Scientifique (CNRS) as a Research Scientist. His current interests concerns the simulation and the optimisation of nanodevices and the development of continuous and atomistic models for silicon process simulation.

Evelyne LAMPIN née MARTIN is in charge of research at the french National Center of Scientific Research (CNRS). She is working at the Institute of Electronic, Microelectronic and Nanotechnology (IEMN) close to Lille. She received the engineer degree from ISEN in 1994 and a PhD degree in Material Science from the University of Lille in 1997. Her dissertation dealt with the calculation of the electronic states and of the dynamic of carriers in silicon nanostructures. She joined the Silicon Microelectronic group of the IEMN in 1997, where she is studying the physics of the advanced silicon technology. Her particular interest is the modeling of dopant diffusion and activation. After developing continuous models of the extended defects formed by ion implantation, she is now using atomistic methods to study the recrystallization of silicon after amorphising implants.

